

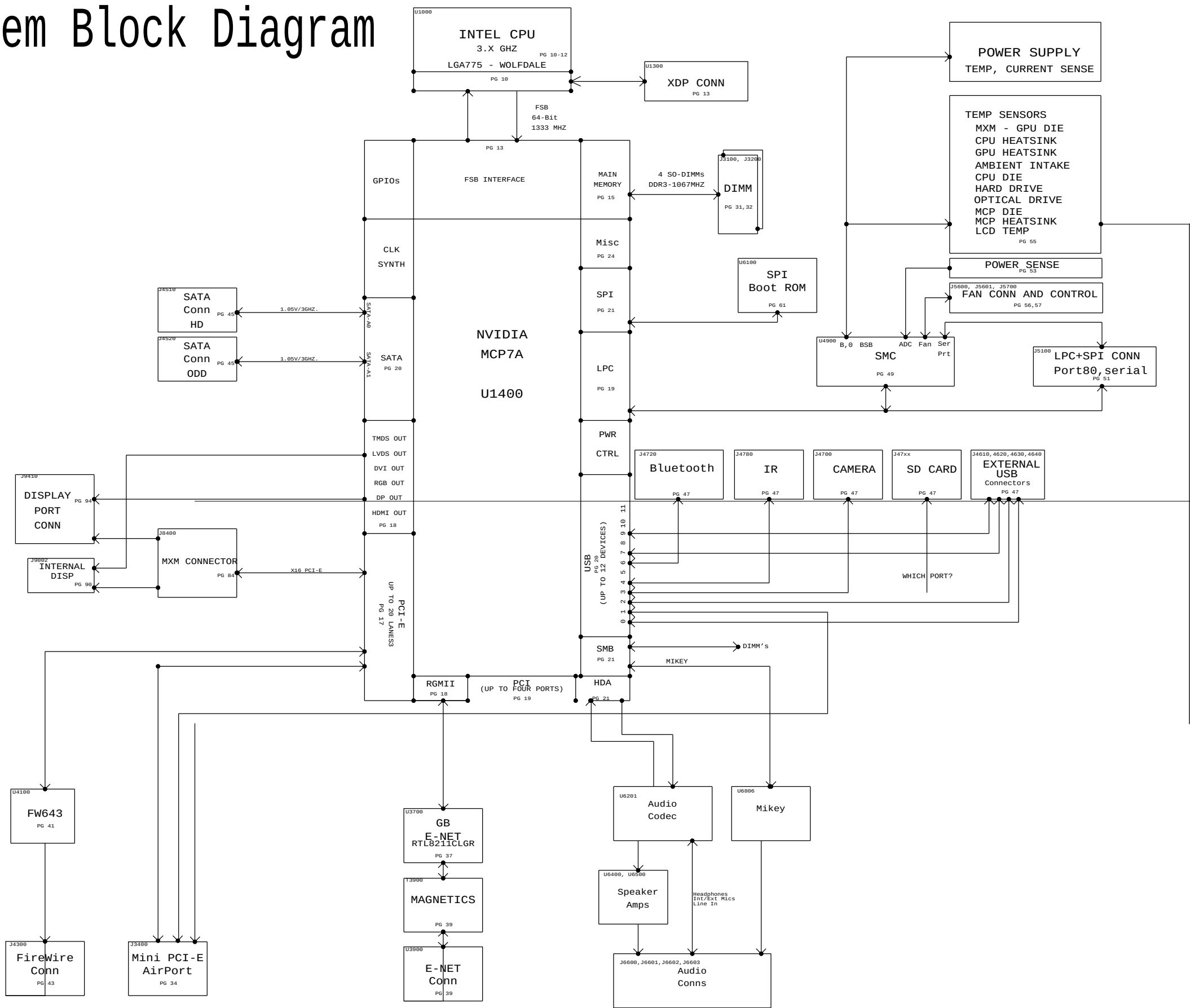
REV	ECN	DESCRIPTION OF REVISION	APPD DATE

Jun 23 2009

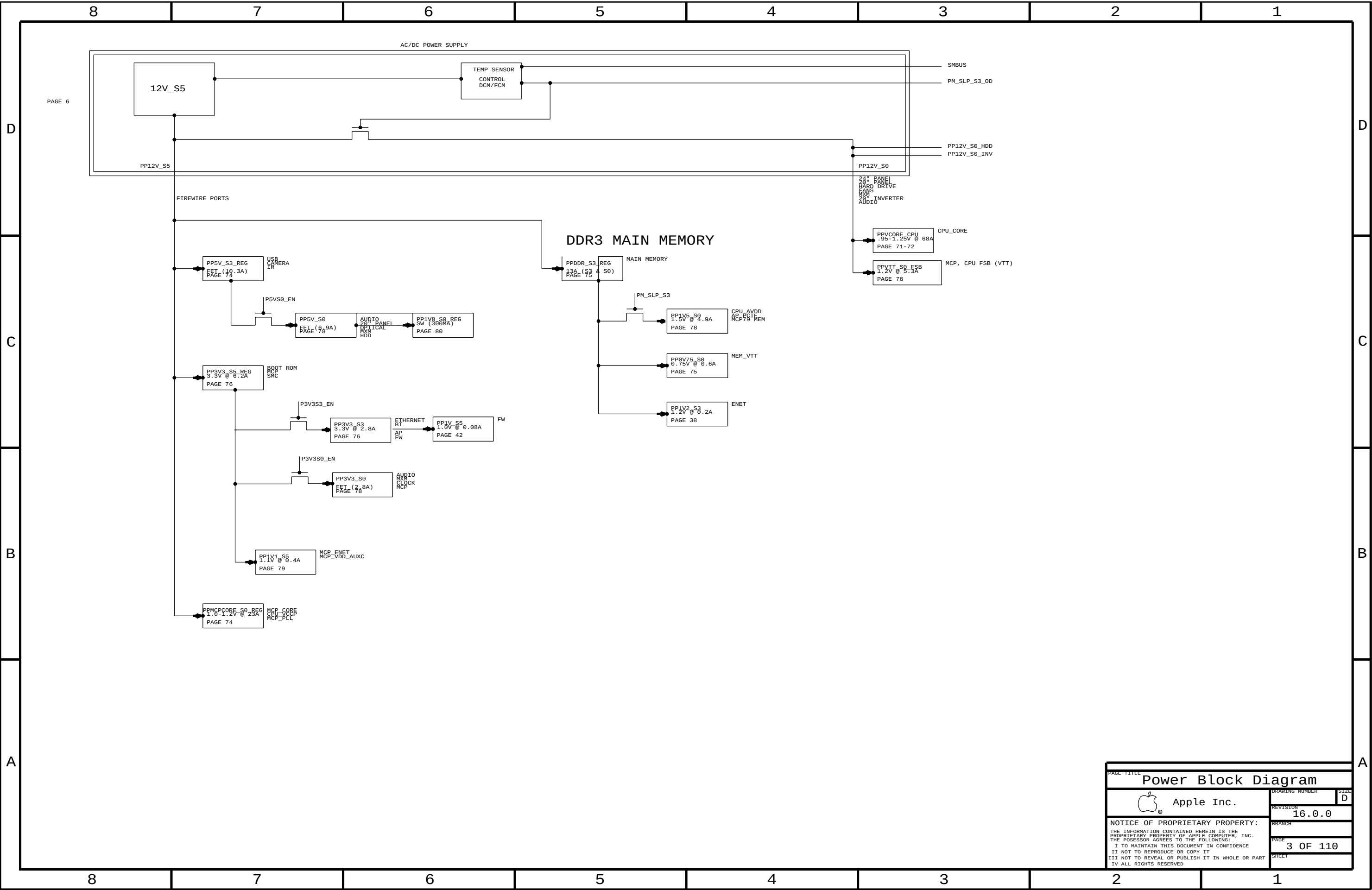
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System Block Diagram



System Block Diagram			
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<table><tr><td>PART#</td><td>QTY</td><td>DESCRIPTION</td><td>REFERENCE DESIGNATOR(S)</td><td>CRITICAL</td><td>BOM OPTION</td></tr><tr><td>820-2567</td><td>1</td><td>PCBF,MLB</td><td>MLB1</td><td></td><td></td></tr></table>								PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	820-2567	1	PCBF,MLB	MLB1						
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION																		
820-2567	1	PCBF,MLB	MLB1																				
BOARD STACK-UP <table><tr><td>TOP</td><td>SIGNAL</td></tr><tr><td>2</td><td>GROUND</td></tr><tr><td>3</td><td>SIGNAL</td></tr><tr><td>4</td><td>POWER</td></tr><tr><td>5</td><td>POWER</td></tr><tr><td>6</td><td>SIGNAL</td></tr><tr><td>7</td><td>GROUND</td></tr><tr><td>BOTTOM</td><td>SIGNAL</td></tr></table>								TOP	SIGNAL	2	GROUND	3	SIGNAL	4	POWER	5	POWER	6	SIGNAL	7	GROUND	BOTTOM	SIGNAL
TOP	SIGNAL																						
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5	POWER																						
6	SIGNAL																						
7	GROUND																						
BOTTOM	SIGNAL																						
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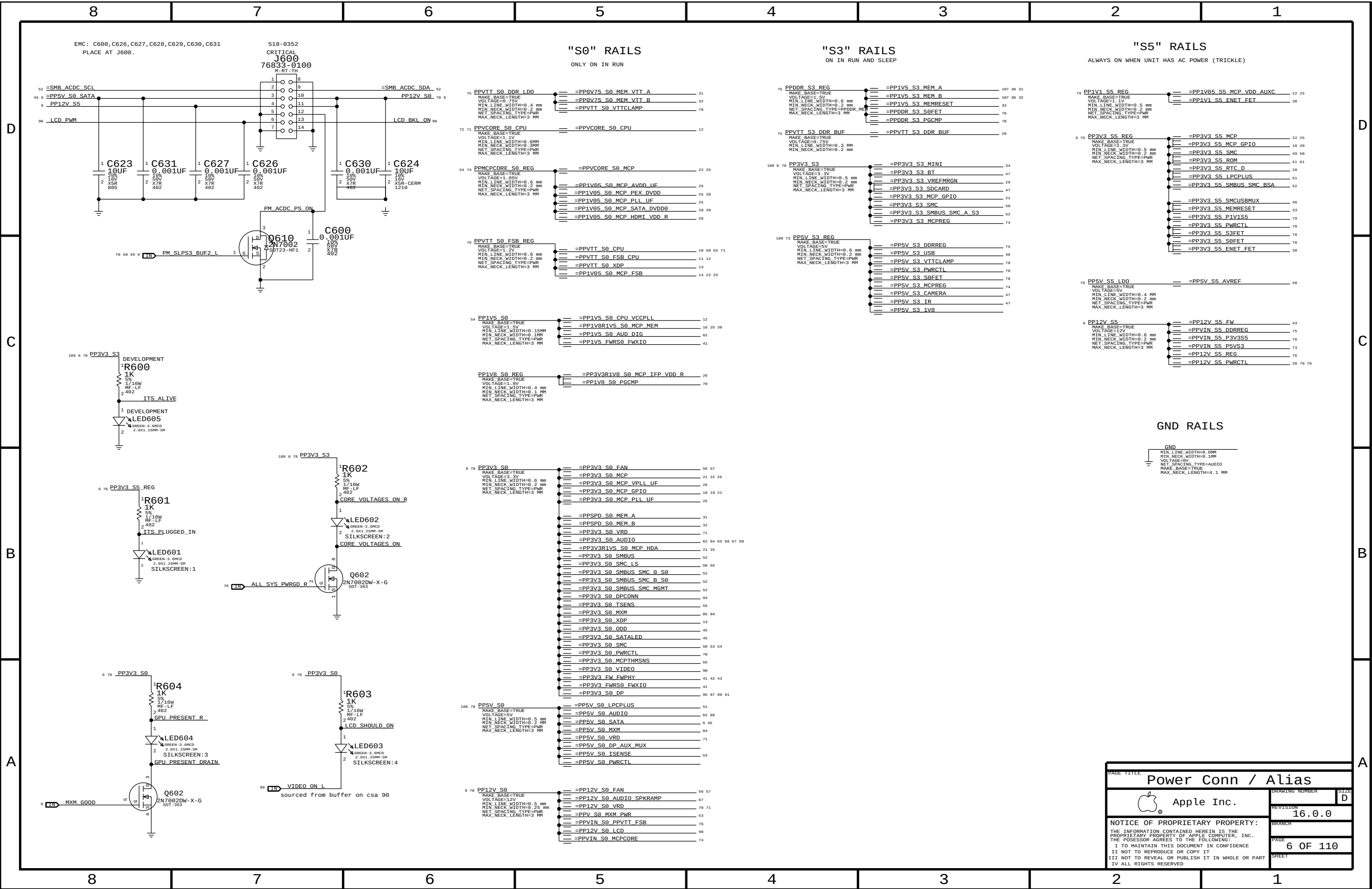
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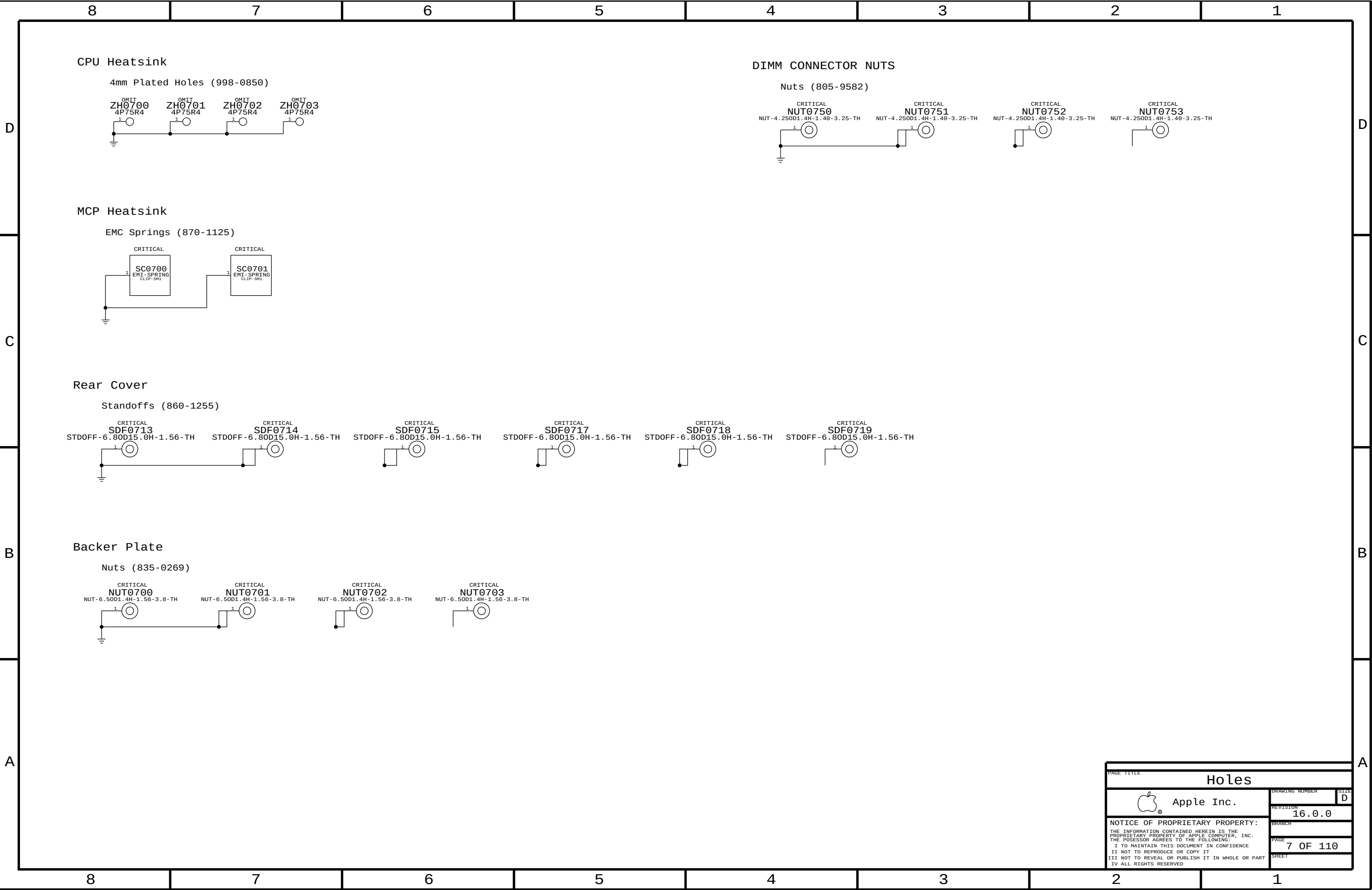
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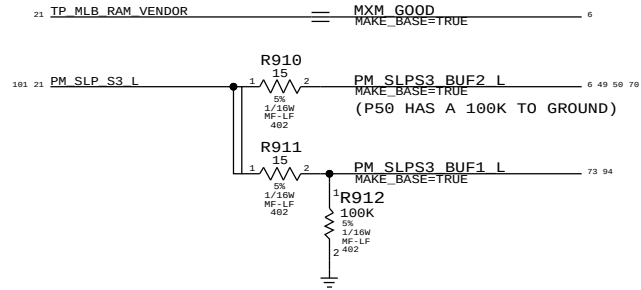




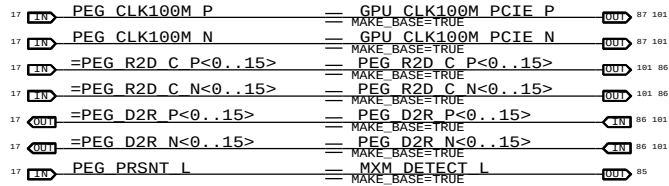
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D	NC ON UNUSED ALIASES						
	18	MCP_TV_DAC_RSET	==	NC_MCP_TV_DAC_RSET	MAKE_BASE=TRUE	NO_TEST=TRUE	
	18	MCP_TV_DAC_VREF	==	NC_MCP_TV_DAC_VREF	MAKE_BASE=TRUE	NO_TEST=TRUE	
	18	MCP_CLK27M_XTALIN	==	NC_MCP_CLK27M_XTALIN	MAKE_BASE=TRUE	NO_TEST=TRUE	
	18	MCP_CLK27M_XTALOUT	==	NC_MCP_CLK27M_XTALOUT	MAKE_BASE=TRUE	NO_TEST=TRUE	
	18	CRT_IG_R_C_PR	==	NC_CRT_IG_R_C_PR	MAKE_BASE=TRUE	NO_TEST=TRUE	
	18	CRT_IG_G_Y_Y	==	NC_CRT_IG_G_Y_Y	MAKE_BASE=TRUE	NO_TEST=TRUE	
	18	CRT_IG_B_COMP_PB	==	NC_CRT_IG_B_COMP_PB	MAKE_BASE=TRUE	NO_TEST=TRUE	
	18	CRT_IG_HSYNC	==	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE	
	18	CRT_IG_VSYNC	==	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE	
C	18	TP_MCP_RGB_HSYNC	==	NC_MCP_RGB_HSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE	
	18	TP_MCP_RGB_VSYNC	==	NC_MCP_RGB_VSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	TP_PCI_AD<31..15>	==	NC_PCI_AD<31..15>	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	TP_PCI_IRDY_L	==	NC_PCI_IRDY_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	TP_PCI_C_BE_L<1..0>	==	NC_PCI_C_BE_L<1..0>	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	TP_PCI_SERR_L	==	NC_PCI_SERR_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	TP_PCI_DEVSEL_L	==	NC_PCI_DEVSEL_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	TP_PCI_PERR_L	==	NC_PCI_PERR_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	TP_LPC_DRQ0_L	==	NC_LPC_DRQ0_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
	21	TP_MCP_BUF_SIO_CLK	==	NC_MCP_BUF_SIO_CLK	MAKE_BASE=TRUE	NO_TEST=TRUE	
B	18	TP_ENET_INTR_L	==	NC_ENET_INTR_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
	18	TP_ENET_PWDWN_L	==	NC_ENET_PWDWN_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
	21	TP_MCP_KBDRSTIN_L	==	NC_MCP_KBDRSTIN_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
	18	TP_MCP_GPIO_18	==	NC_MCP_GPIO_18	MAKE_BASE=TRUE	NO_TEST=TRUE	
	21	TP_MLB_RAM_SIZE	==	NC_MLB_RAM_SIZE	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	TP_PCI_C_BE_L<3>	==	NC_PCI_C_BE_L<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	TP_PCI_CLK0	==	NC_PCI_CLK0	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	TP_PCI_CLK1	==	NC_PCI_CLK1	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	TP_PCI_FRAME_L	==	NC_PCI_FRAME_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	TP_PCI_GNT0_L	==	NC_MCP_PCI_GNT0_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
A	19	TP_PCI_GNT1_L	==	NC_PCI_GNT1_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	TP_PCI_INTW_L	==	NC_PCI_INTW_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	TP_PCI_INTX_L	==	NC_PCI_INTX_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	TP_PCI_INTY_L	==	NC_PCI_INTY_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	TP_PCI_INTZ_L	==	NC_PCI_INTZ_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	TP_PCI_PAR	==	NC_PCI_PAR	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	TP_PCI_RESET1_L	==	NC_PCI_RESET1_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	TP_PCI_STOP_L	==	NC_PCI_STOP_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	TP_PCI_TRDY_L	==	NC_PCI_TRDY_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
	17	TP_PCIE_CLK100M_PE4N	==	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE	NO_TEST=TRUE	
	17	TP_PCIE_CLK100M_PE4P	==	NC_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE	NO_TEST=TRUE	
	17	TP_PCIE_CLK100M_PE5N	==	NC_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE	NO_TEST=TRUE	
	17	TP_PCIE_CLK100M_PE5P	==	NC_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE	NO_TEST=TRUE	
	17	TP_PCIE_CLK100M_PE6P	==	NC_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE	NO_TEST=TRUE	
	17	TP_PCIE_CLK100M_PE6N	==	NC_PCIE_CLK100M_PE6N	MAKE_BASE=TRUE	NO_TEST=TRUE	
	17	PCIE_EXCARD_PRSNT_L	==	NC_PCIE_EXCARD_PRSNT_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
	17	TP_PE4_CLKREQ_L	==	NC_PE4_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
	17	TP_PE4_PRSNT_L	==	NC_PE4_PRSNT_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
	21	TP_SB_A20GATE	==	NC_SB_A20GATE	MAKE_BASE=TRUE	NO_TEST=TRUE	
	20	TP_USB_10N	==	NC_USB_10N	MAKE_BASE=TRUE	NO_TEST=TRUE	
	20	TP_USB_10P	==	NC_USB_10P	MAKE_BASE=TRUE	NO_TEST=TRUE	
	20	USB_MINI_N	==	NC_USB_MINI_N	MAKE_BASE=TRUE	NO_TEST=TRUE	
	20	USB_MINI_P	==	NC_USB_MINI_P	MAKE_BASE=TRUE	NO_TEST=TRUE	
	20	USB_EXCARD_N	==	NC_USB_EXCARD_N	MAKE_BASE=TRUE	NO_TEST=TRUE	
	20	USB_EXCARD_P	==	NC_USB_EXCARD_P	MAKE_BASE=TRUE	NO_TEST=TRUE	
	21	ODD_PWR_EN_L	==	NC_ODD_PWR_EN_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
	17	PCIE_CLK100M_EXCARD_P	==	NC_PCIE_CLK100M_EXCARD_P	MAKE_BASE=TRUE	NO_TEST=TRUE	
	17	PCIE_CLK100M_EXCARD_N	==	NC_PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE	NO_TEST=TRUE	
	17	EXCARD_CLKREQ_L	==	NC_EXCARD_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	TP_PCI_AD<12..10>	==	NC_PCI_AD<12..10>	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	TP_PCI_AD<8>	==	NC_PCI_AD<8>	MAKE_BASE=TRUE	NO_TEST=TRUE	
	17	TP_PCIE_PE4_R2D_CP	==	NC_PCIE_PE4_R2D_CP	MAKE_BASE=TRUE	NO_TEST=TRUE	
	17	TP_PCIE_PE4_R2D_CN	==	NC_PCIE_PE4_R2D_CN	MAKE_BASE=TRUE	NO_TEST=TRUE	
	17	TP_PCIE_PE4_D2RP	==	NC_PCIE_PE4_D2RP	MAKE_BASE=TRUE	NO_TEST=TRUE	
	17	TP_PCIE_PE4_D2RN	==	NC_PCIE_PE4_D2RN	MAKE_BASE=TRUE	NO_TEST=TRUE	
	17	PCIE_EXCARD_D2R_P	==	NC_PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE	NO_TEST=TRUE	
	17	PCIE_EXCARD_D2R_N	==	NC_PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE	NO_TEST=TRUE	
	17	PCIE_EXCARD_R2D_C_P	==	NC_PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE	NO_TEST=TRUE	
	17	PCIE_EXCARD_R2D_C_N	==	NC_PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE	NO_TEST=TRUE	
	20	USB_TPAD_N	==	NC_USB_TPAD_N	MAKE_BASE=TRUE	NO_TEST=TRUE	
	20	USB_TPAD_P	==	NC_USB_TPAD_P	MAKE_BASE=TRUE	NO_TEST=TRUE	
	MCP HAS INTERNAL 15K PULL-DOWNS						
	UNUSED MEMORY SIGNALS						
	15	TP_MEM_A_CLK2P	==	NC_MEM_A_CLK2P	MAKE_BASE=TRUE	NO_TEST=TRUE	
	15	TP_MEM_A_CLK2N	==	NC_MEM_A_CLK2N	MAKE_BASE=TRUE	NO_TEST=TRUE	
	16	TP_MEM_A_CLK5P	==	NC_MEM_A_CLK5P	MAKE_BASE=TRUE	NO_TEST=TRUE	
	16	TP_MEM_A_CLK5N	==	NC_MEM_A_CLK5N	MAKE_BASE=TRUE	NO_TEST=TRUE	
	15	TP_MEM_B_CLK2P	==	NC_MEM_B_CLK2P	MAKE_BASE=TRUE	NO_TEST=TRUE	
	15	TP_MEM_B_CLK2N	==	NC_MEM_B_CLK2N	MAKE_BASE=TRUE	NO_TEST=TRUE	
	16	TP_MEM_B_CLK5P	==	NC_MEM_B_CLK5P	MAKE_BASE=TRUE	NO_TEST=TRUE	
	16	TP_MEM_B_CLK5N	==	NC_MEM_B_CLK5N	MAKE_BASE=TRUE	NO_TEST=TRUE	
	UNUSED GMUX JTAG FROM MCP						
	17	GMUX_JTAG_TCK_L	==	NC_GMUX_JTAG_TCK_L	MAKE_BASE=TRUE	NO_TEST=TRUE	
	17	GMUX_JTAG_TDO	==	NC_GMUX_JTAG_TDO	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	GMUX_JTAG_TDI	==	NC_GMUX_JTAG_TDI	MAKE_BASE=TRUE	NO_TEST=TRUE	
	19	GMUX_JTAG_TMS	==	NC_GMUX_JTAG_TMS	MAKE_BASE=TRUE	NO_TEST=TRUE	
	UNUSED SIGNAL ALIAS						
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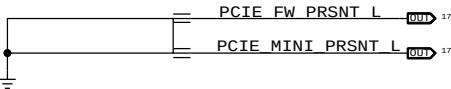
SIGNAL ALIAS



PEG Slot Support

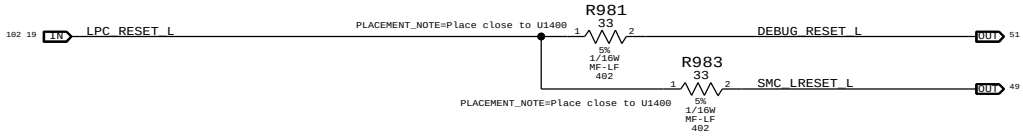


K22/K23 Use one GPIO for both ports 2&3 OC
USB PORT 2 AND 3 (C AND D) SHARE OVER-CURRENT WITH PORT 2
PREVIOUSLY, PORT 3 HAD IT'S OWN BUT EFI MAPS THAT TO EXPRESSCARD
SEE RDAR://6250424

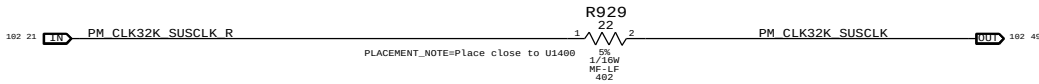
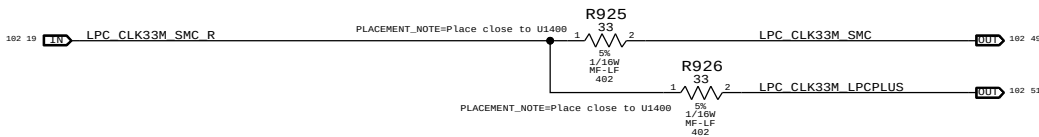
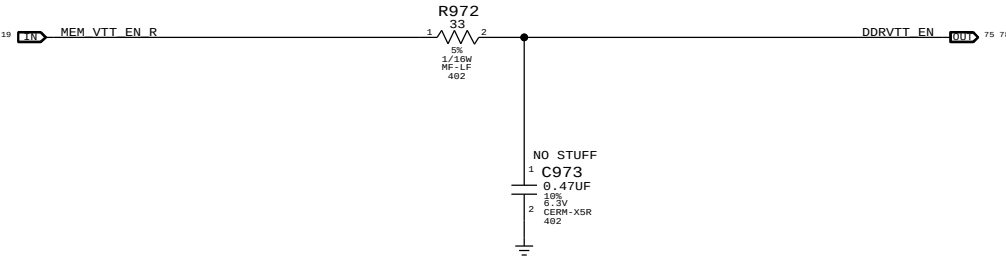
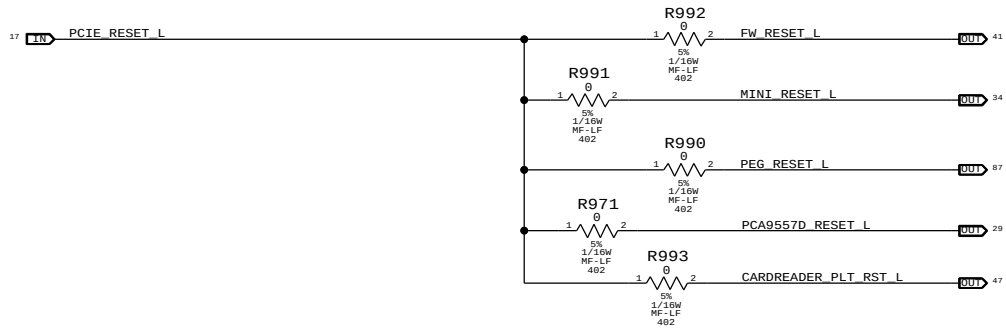


Platform Reset Connections

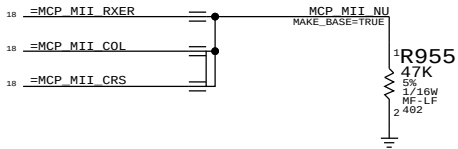
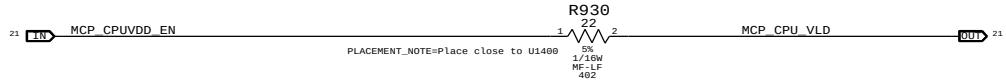
LPC Reset (Unbuffered)



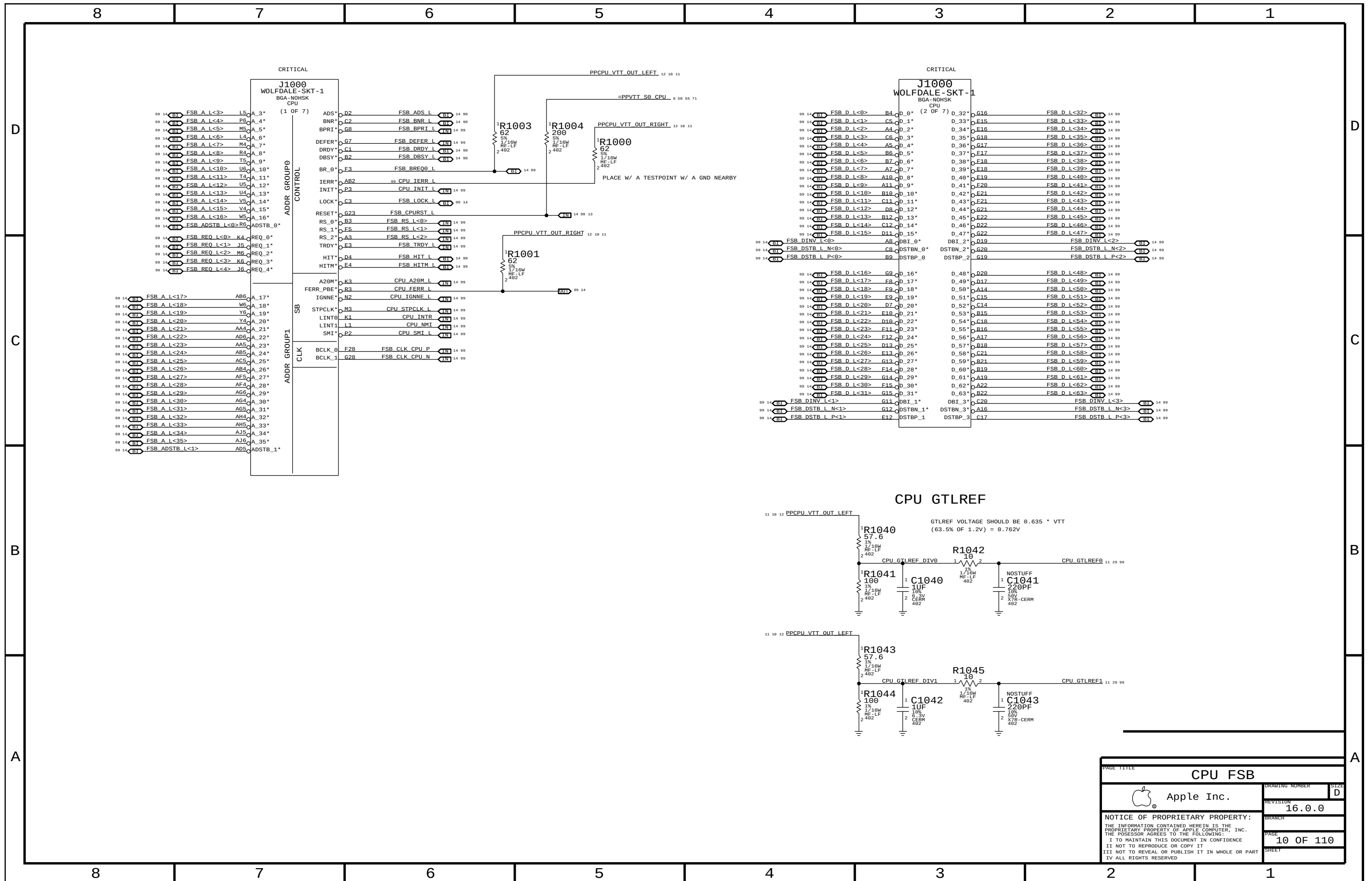
PCIE Reset (Unbuffered)

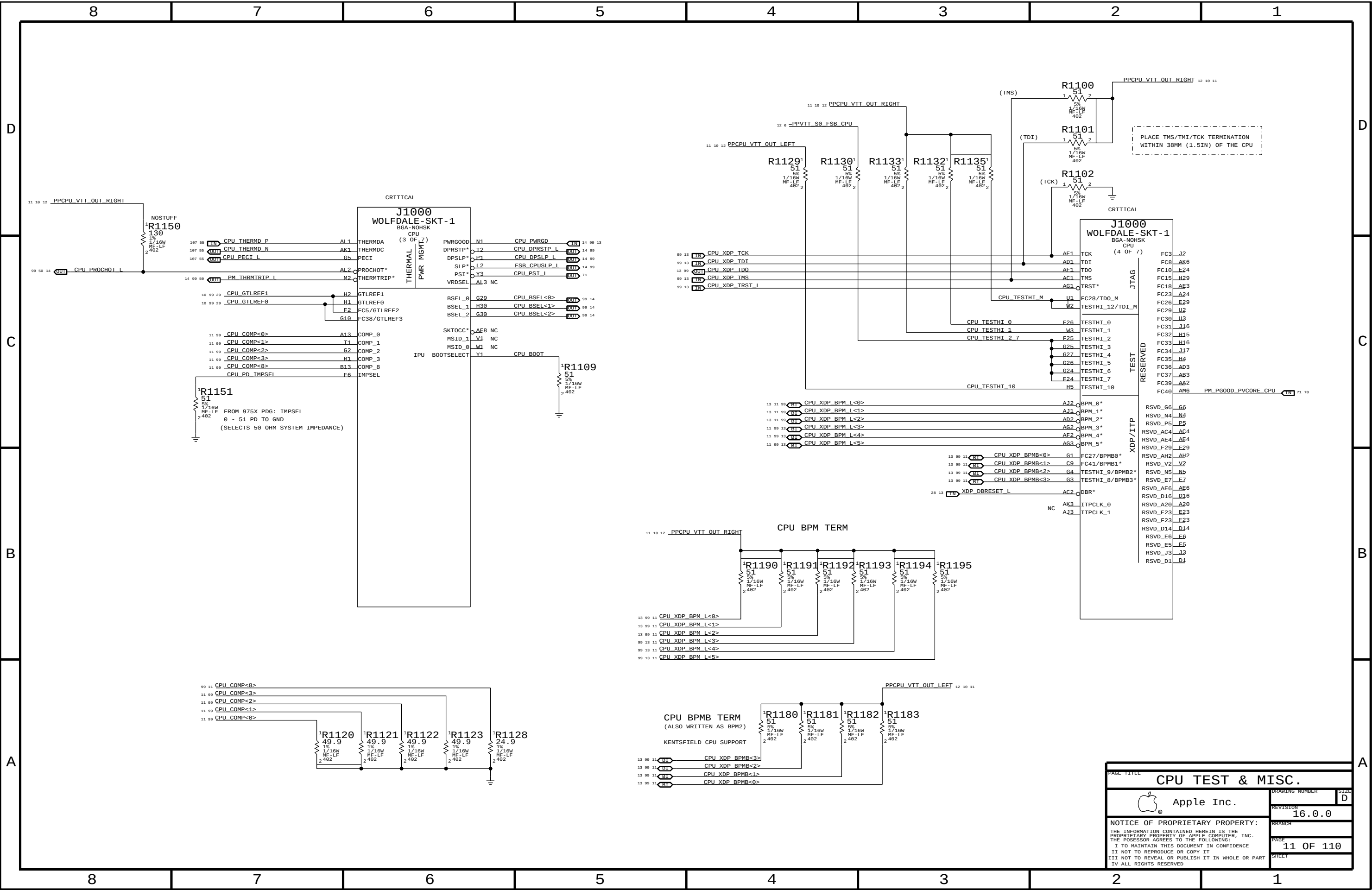


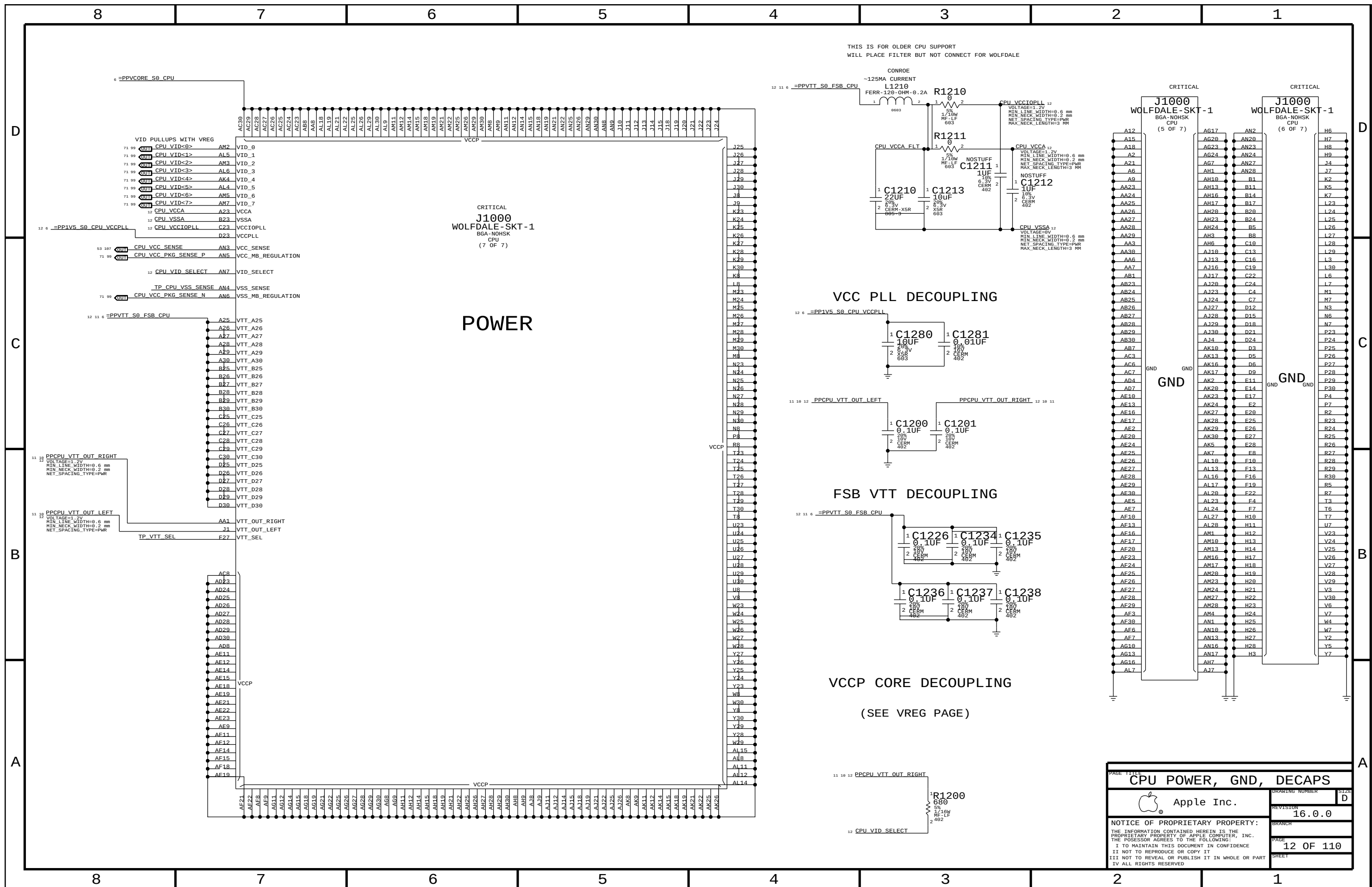
MCP_CPUVDD_EN WILL ASSERT AFTER MCP_PS_PWRGD IS UP



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The schematic diagram illustrates the XDP connector (J1300) and its connections to various components. The connector is labeled "XDP_CONN CRITICAL J1300 LTH-030-01-G-D-A-TR F-ST-SM".

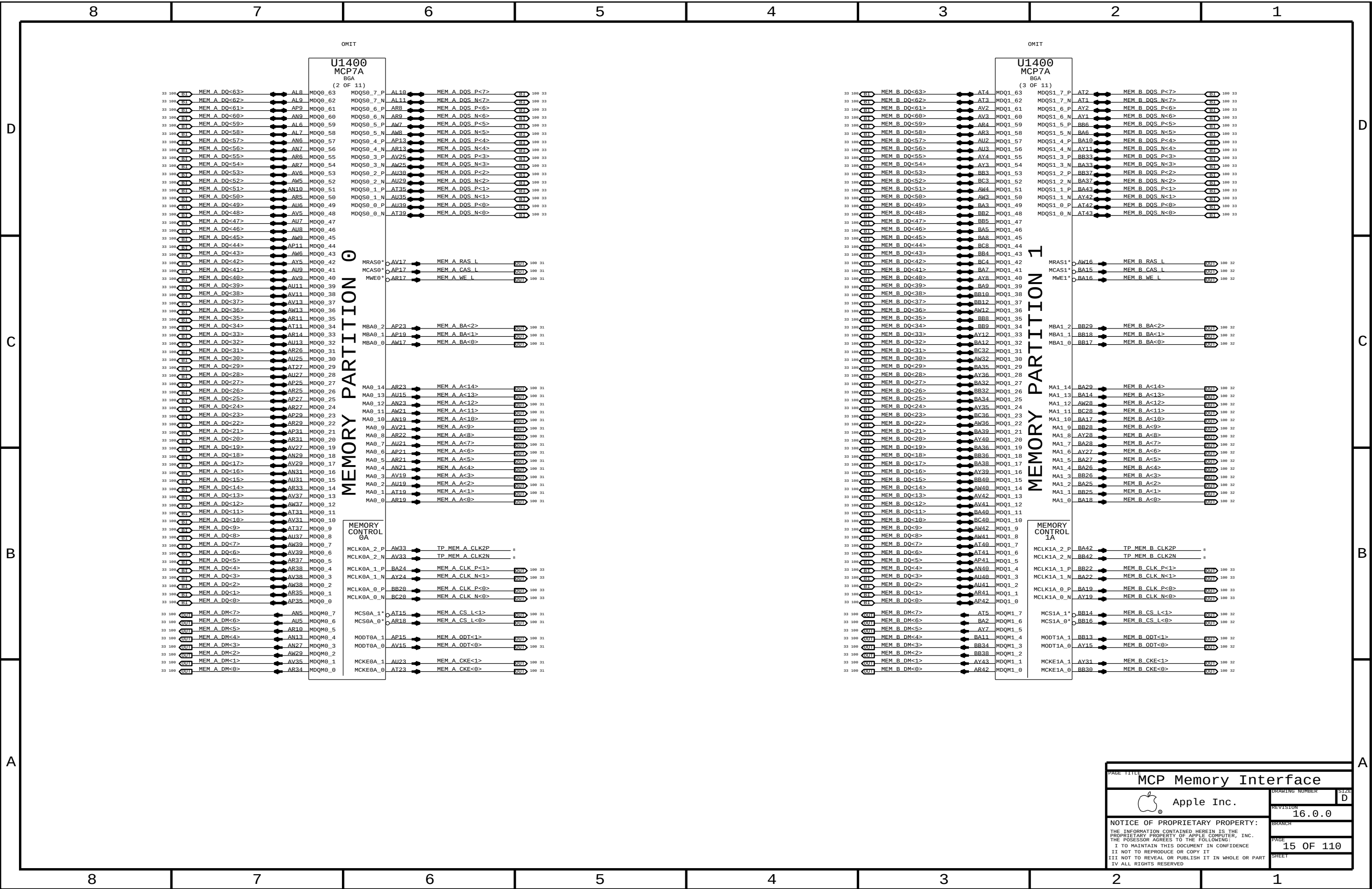
Connections and Components:

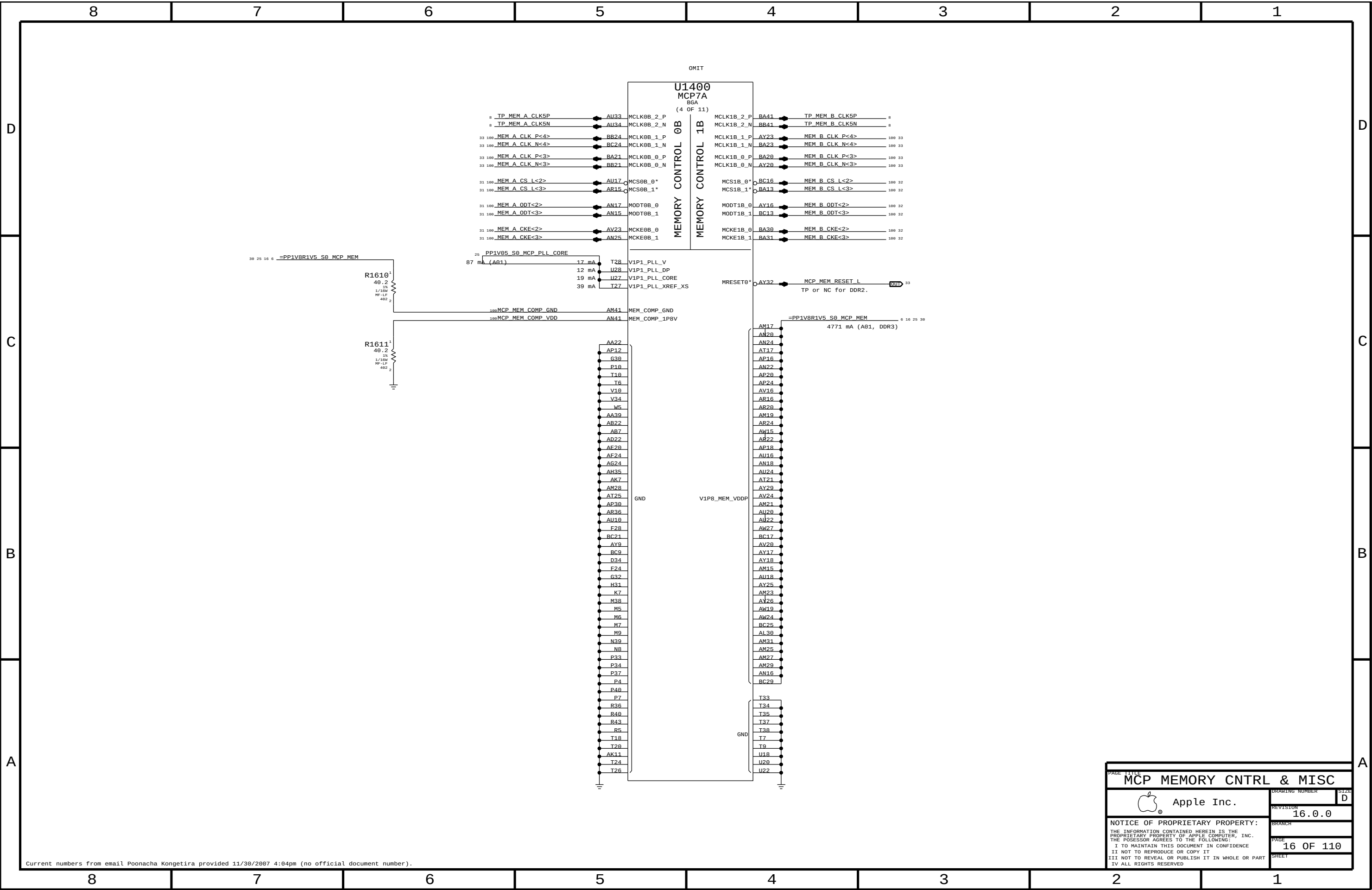
- Top Connections:**
 - XDP:** Connected to **R1315** (54.9, 1%, 1/16W, MF-LF, 402) and **R1301** (51, 1%, 1/16W, MF-LF, 402).
 - PP3V3_S0_XDP** and **PPVTT_S0_XDP** are connected to the top of the connector.
- Left Connections:**
 - CPU XDP:** Multiple lines for **BPM** (L<5>, L<4>, L<3>, L<2>, L<1>, L<0>) and **BPMB** (L<3>, L<2>, L<1>, L<0>).
 - TP XDP:** **OBSFN_B0** and **OBSFN_B1**.
 - PM LATRIGGER_L** and **JTAG MCP TCK** are connected to **PM** and **OUT** pins.
 - SMBUS MCP_0_DATA** and **SMBUS MCP_0_CLK** are connected to **52** and **105** pins.
 - CPU XDP TCK** is connected to **11** and **99** pins.
- Right Connections:**
 - JTAG MCP:** **TD0**, **TRST_L**, **TDI**, and **TMS**.
 - MCP DEBUG:** Multiple lines for **0** through **7**.
 - FSB CLK ITP P** and **FSB CLK ITP N** are connected to **14** and **99** pins.
 - FSB CPURST_L** is connected to **14** and **99** pins.
- Internal Connections:**
 - OBSFN_A0** through **OBSFN_D1** are connected to **2** through **25** pins.
 - OBSDATA_A0** through **OBSDATA_D3** are connected to **10** through **37** pins.
 - WAKE#** is connected to **40** and **41** pins.
 - NCX** is connected to **58** and **59** pins.
- Other Components:**
 - R1399** (1K, 1%, 1/16W, MF-LF, 402) is connected to **CPU PWRGD** and **XDP PWRGD**.
 - R1303** (1K, 1%, 1/16W, MF-LF, 402) is connected to **XDP OBS20** and **FSB CPURST_L**.
 - C1300** (0.1uF, 10%, 10V, XSR, 402) is connected to **XDP** and **XDP OBS20**.
 - C1301** (0.1uF, 10%, 10V, XSR, 402) is connected to **XDP** and **XDP DBRESET_L**.

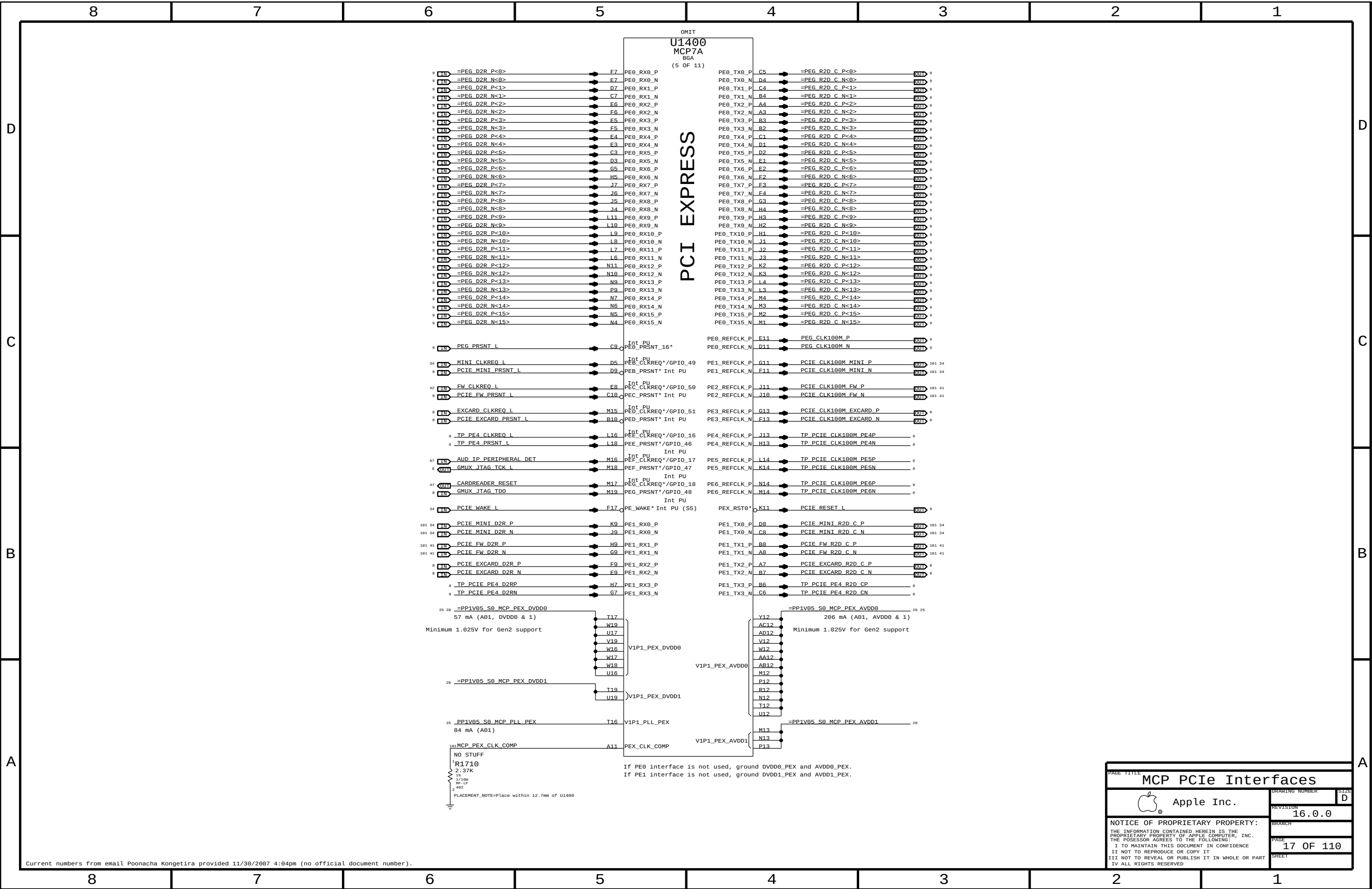
Note: XDP_DBRESET_L must be pulled-up to 3.3V.

Placement Note: Place close to CPU to minimize stub.

PART TITLE		DRAWING NUMBER		SIZE	
extended Debug Port (XDP)				D	
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PAGE TITLE

MCP PCIe Interfaces

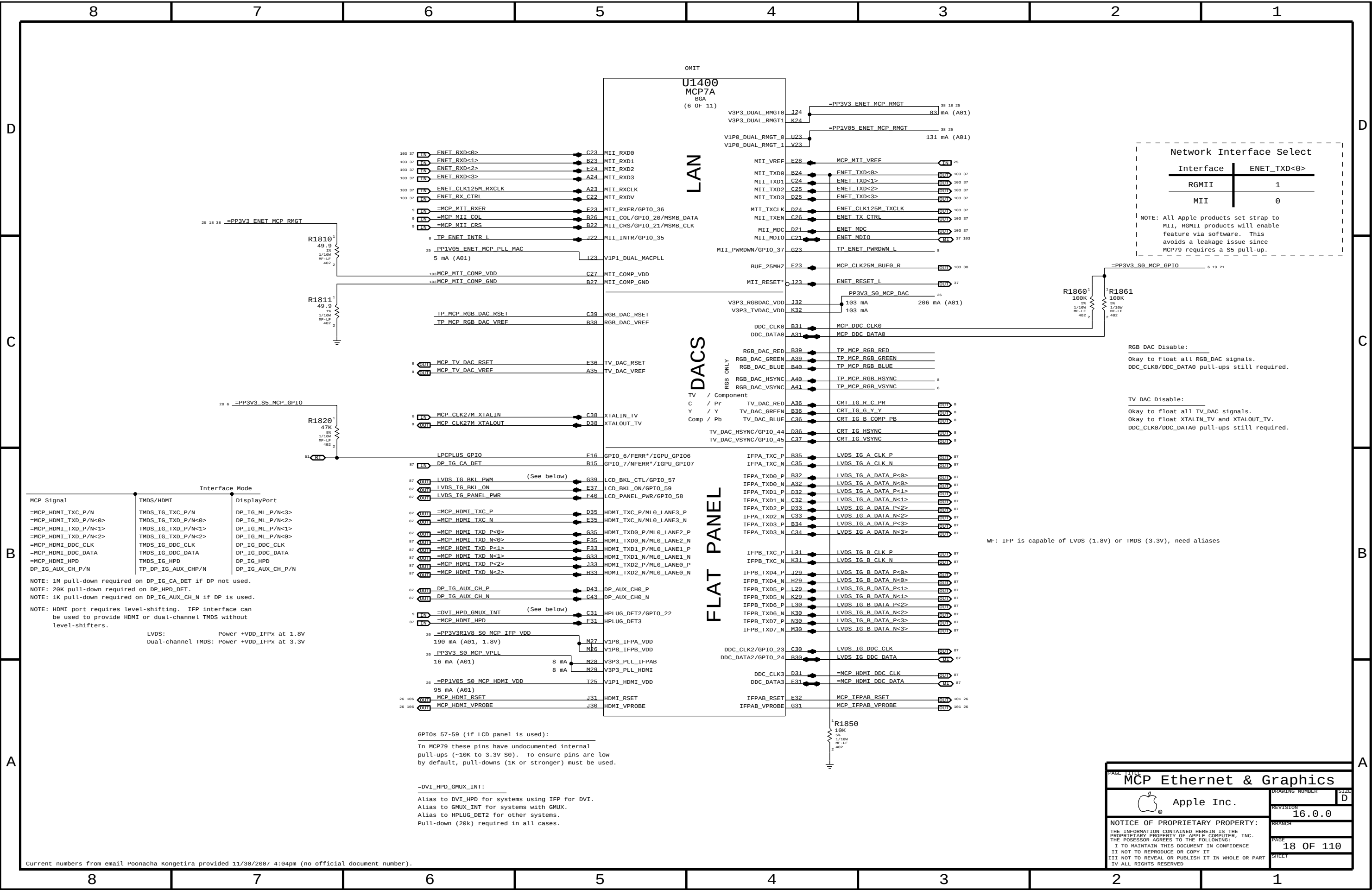
Apple Inc.

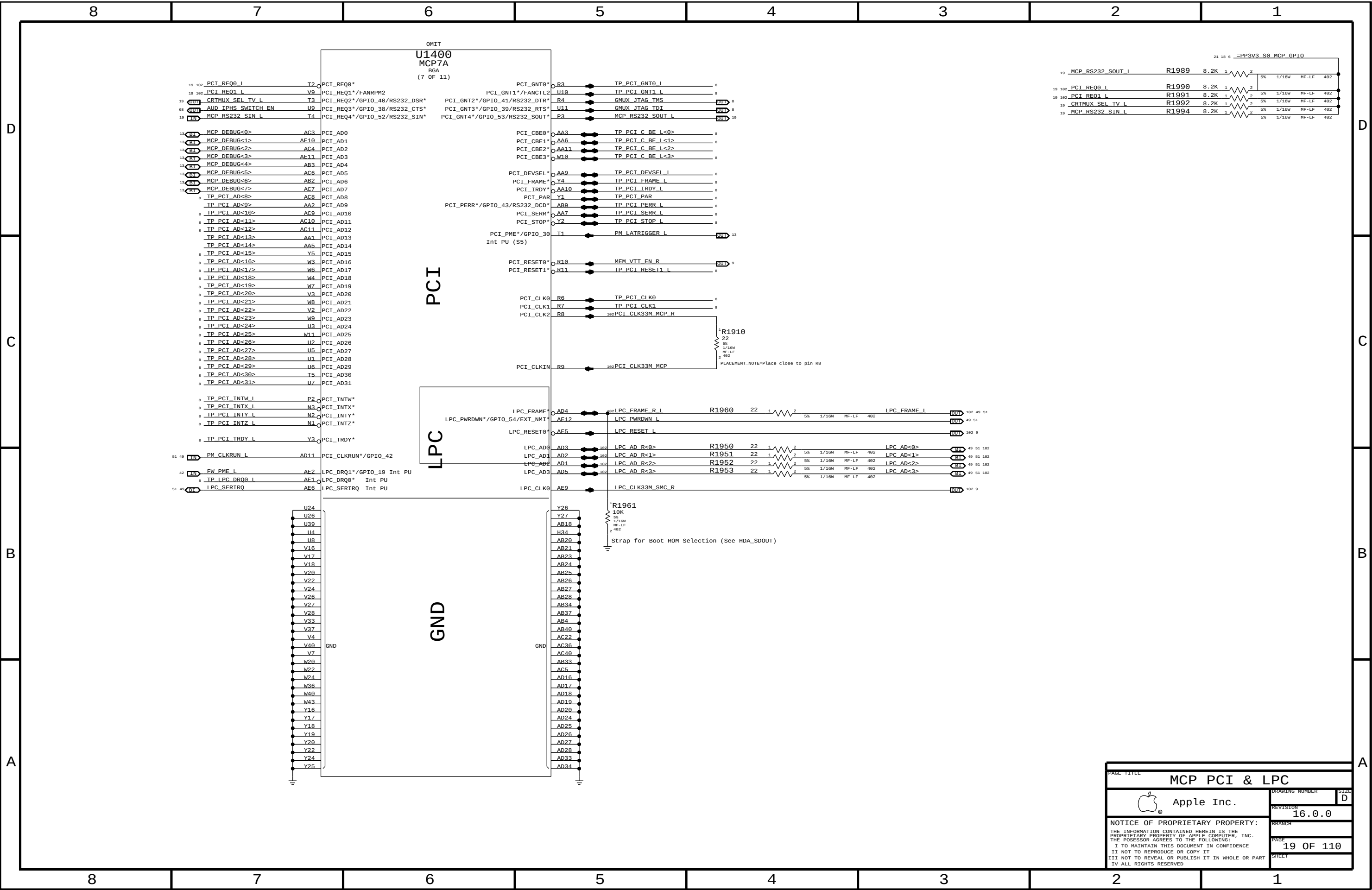
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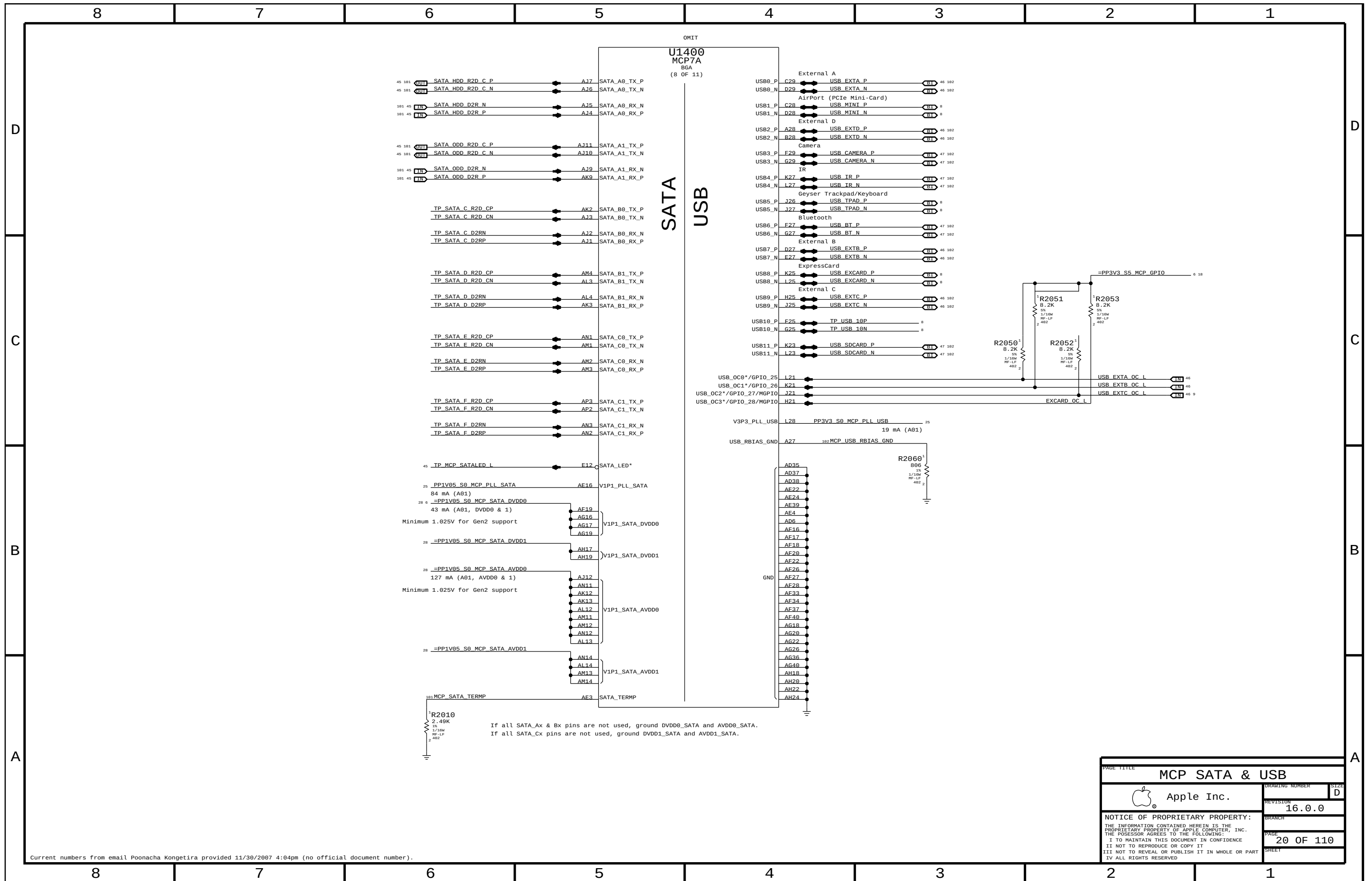
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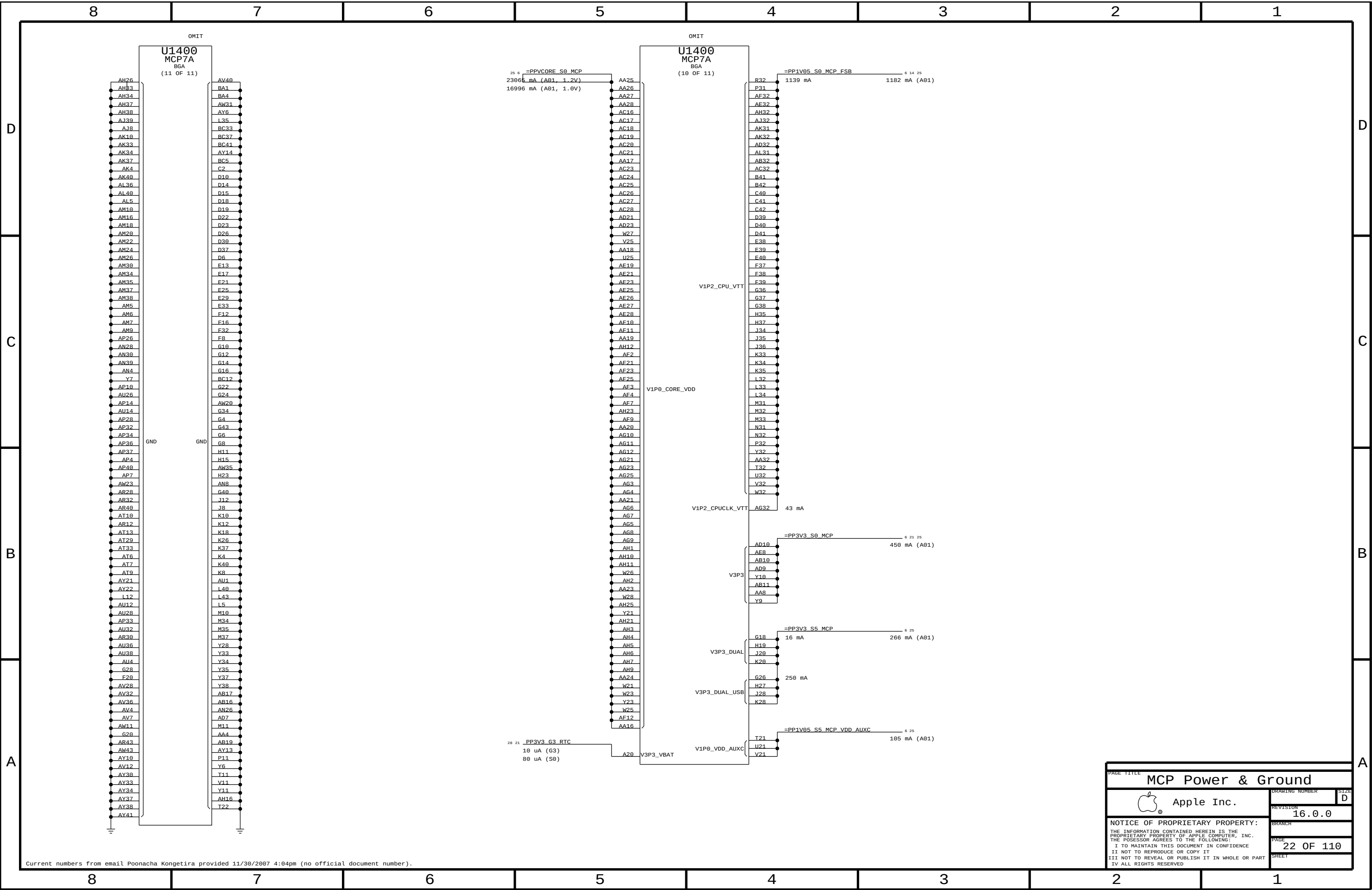
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SIZE
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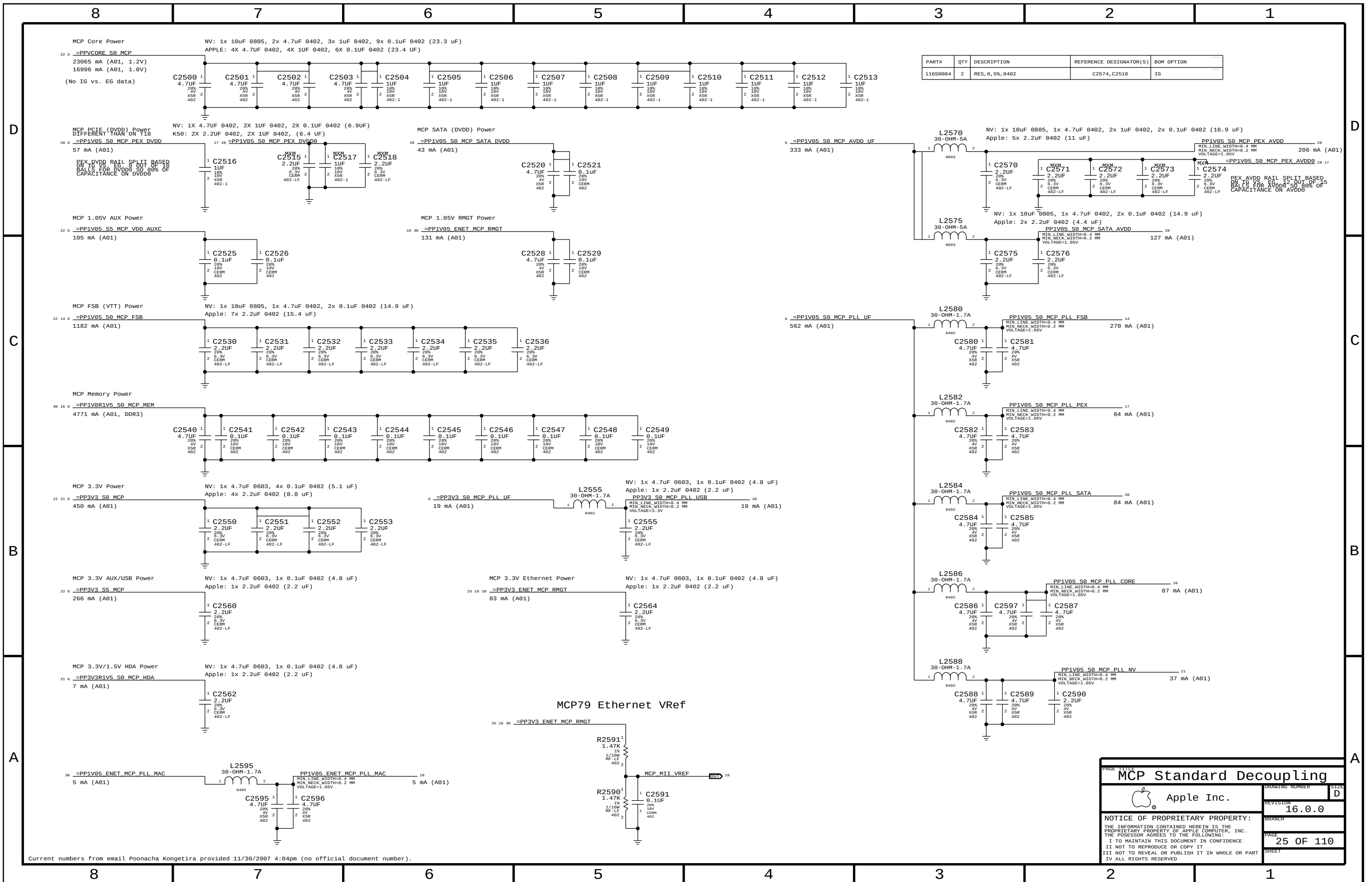


PAGE TITLE		MCP Power & Ground	
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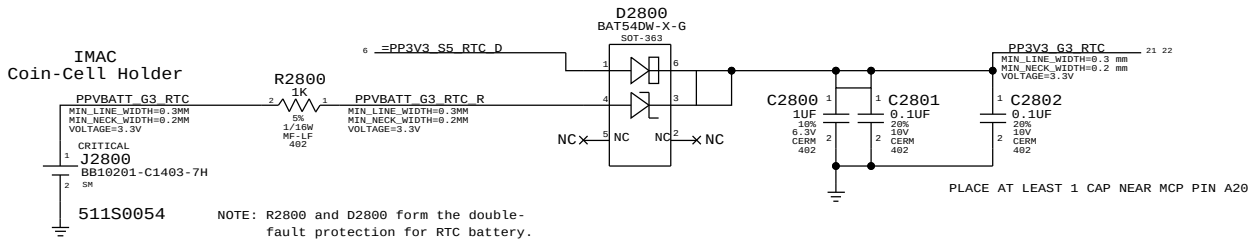
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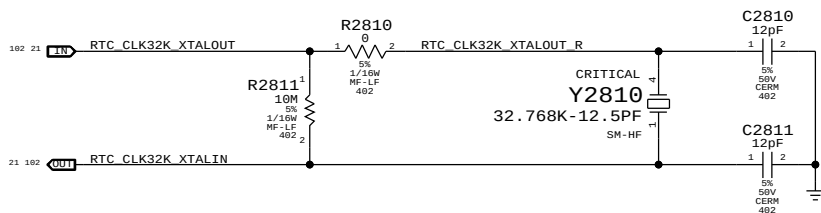
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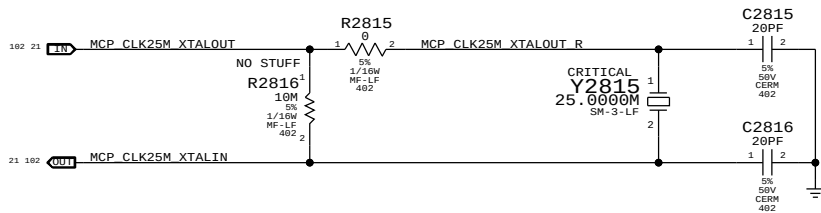
RTC Power Sources



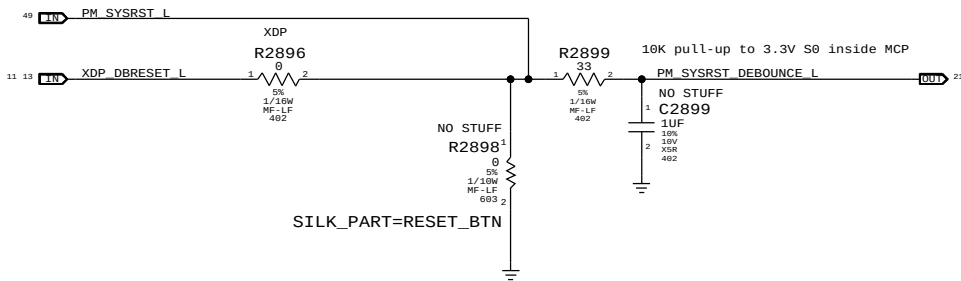
RTC Crystal



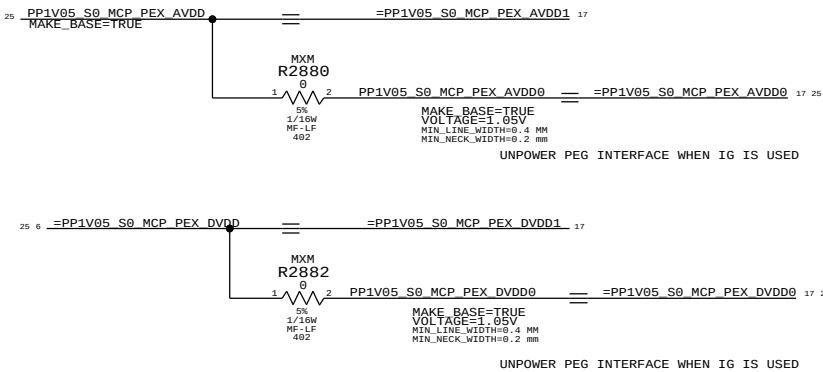
MCP 25MHz Crystal



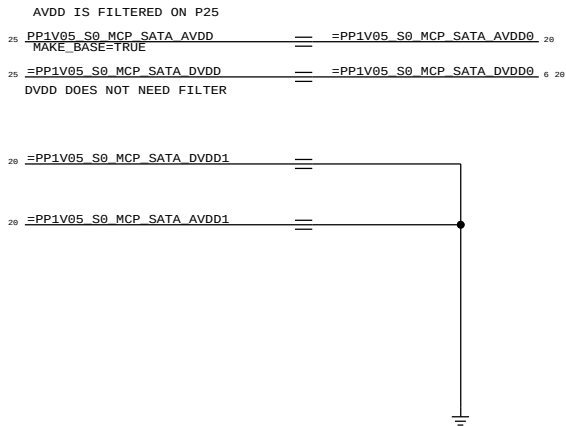
Reset Button



PEG POWER ALIAS/OPTION TO GND UNUSED POWER PIN



SATA ALIAS/GROUNDING UNUSED DVDD1 AND AVDD1



Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
PRODUCTION

DAC channel
Min DAC code
Max DAC code
Max sink I
Max source I
Nominal Vref
Min Vref
Max Vref
Vref Stepping
(per DAC LSB)

MEM A VREF DQ
A
0x00
0x87
-3.75 mA
5 mA
0.75 V
0.375 V
1.250 V
6.5 mV

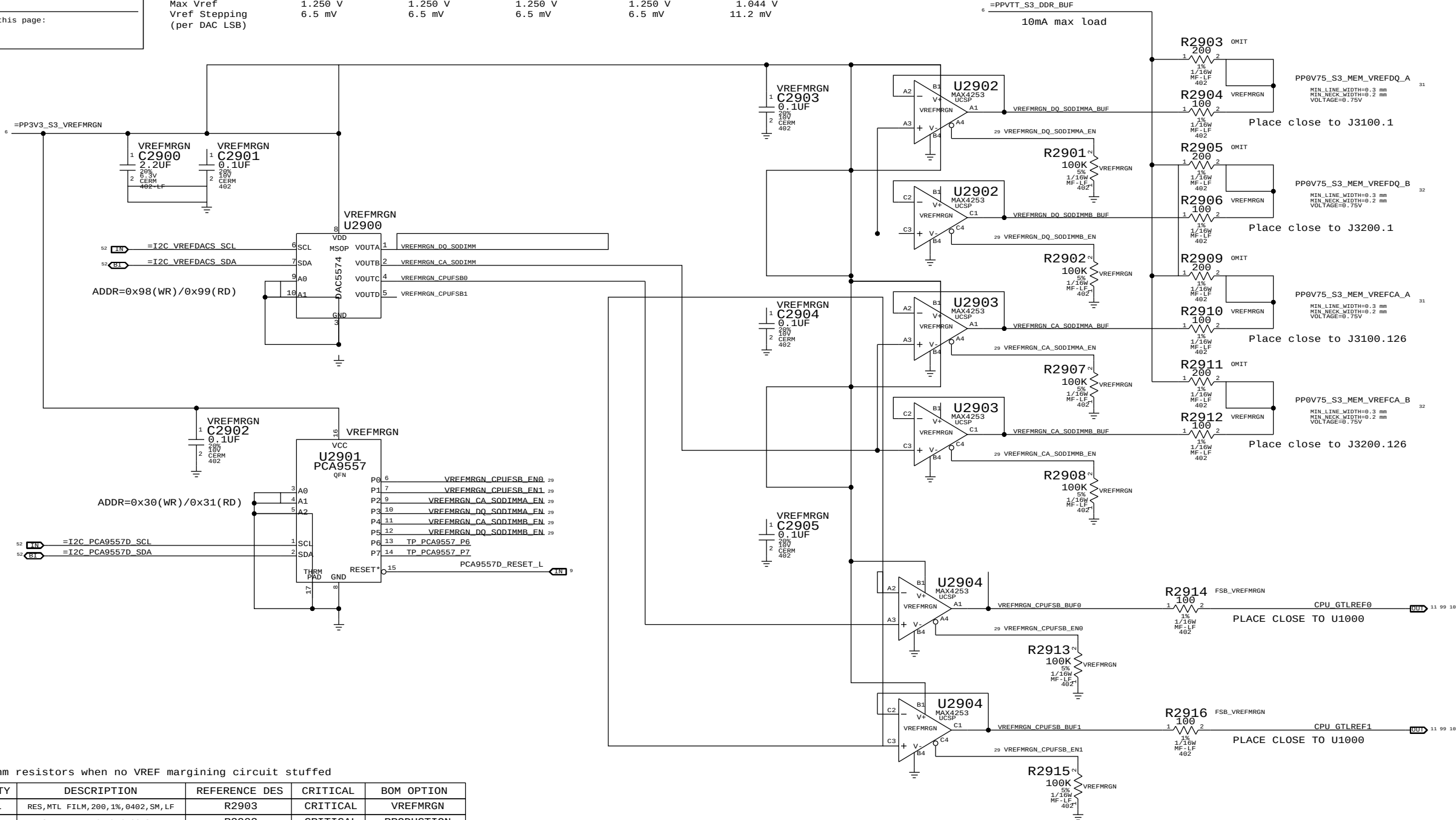
MEM A VREF CA
B
0x00
0x87
-3.75 mA
5 mA
0.75 V
0.375 V
1.250 V
6.5 mV

MEM B VREF DQ
A
0x00
0x87
-3.75 mA
5 mA
0.75 V
0.375 V
1.250 V
6.5 mV

MEM B VREF CA
B
0x00
0x87
-3.75 mA
5 mA
0.75 V
0.375 V
1.250 V
6.5 mV

CPU FSB VREF
C
0x00
0x55
-0.91 mA
0.52 mA
0.70 V
0.091 V
1.044 V
11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2903	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2905	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2909	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2911	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	PRODUCTION

PAGE TITLE

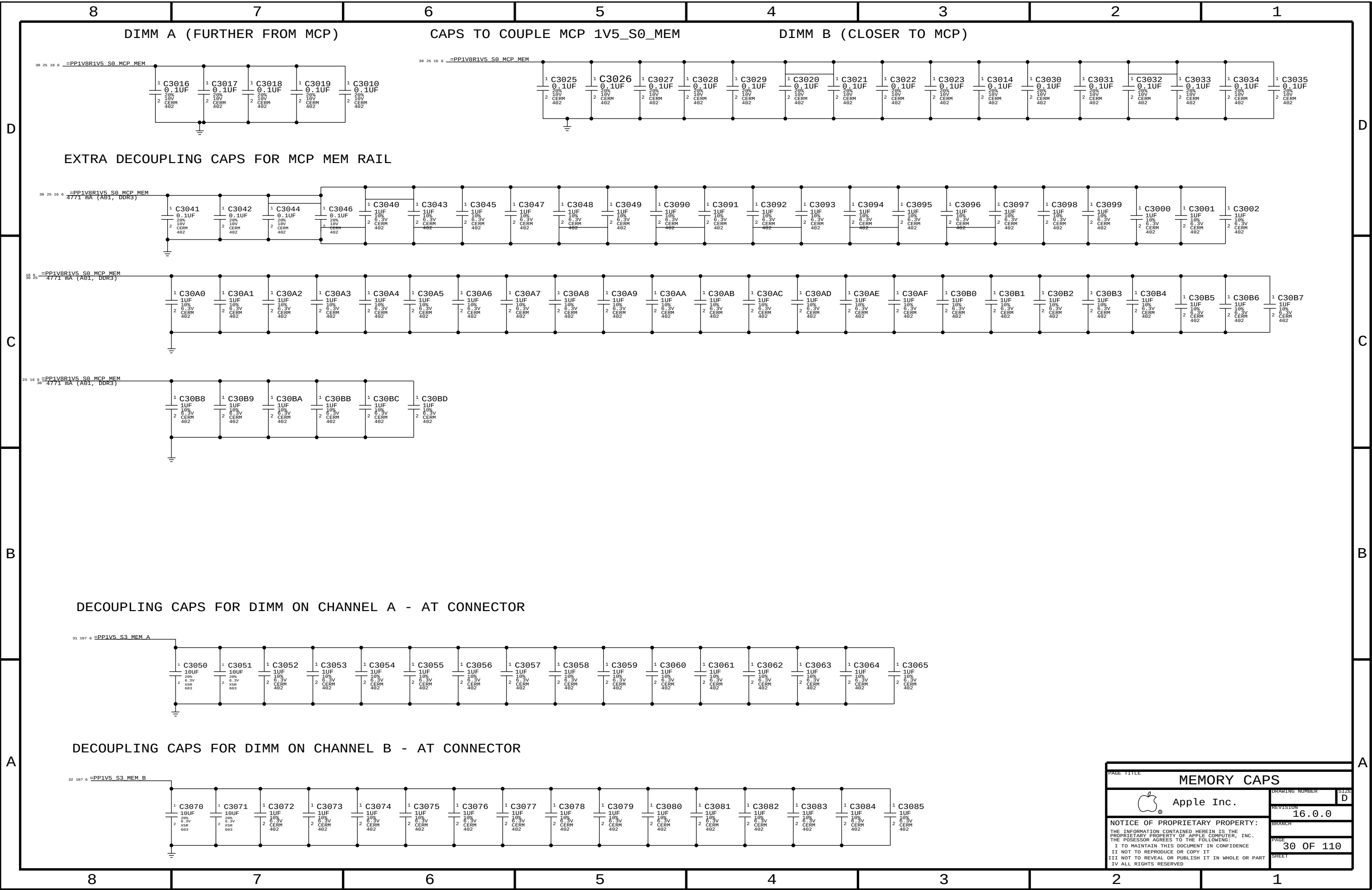
FSB/DDR3 Vref Margining

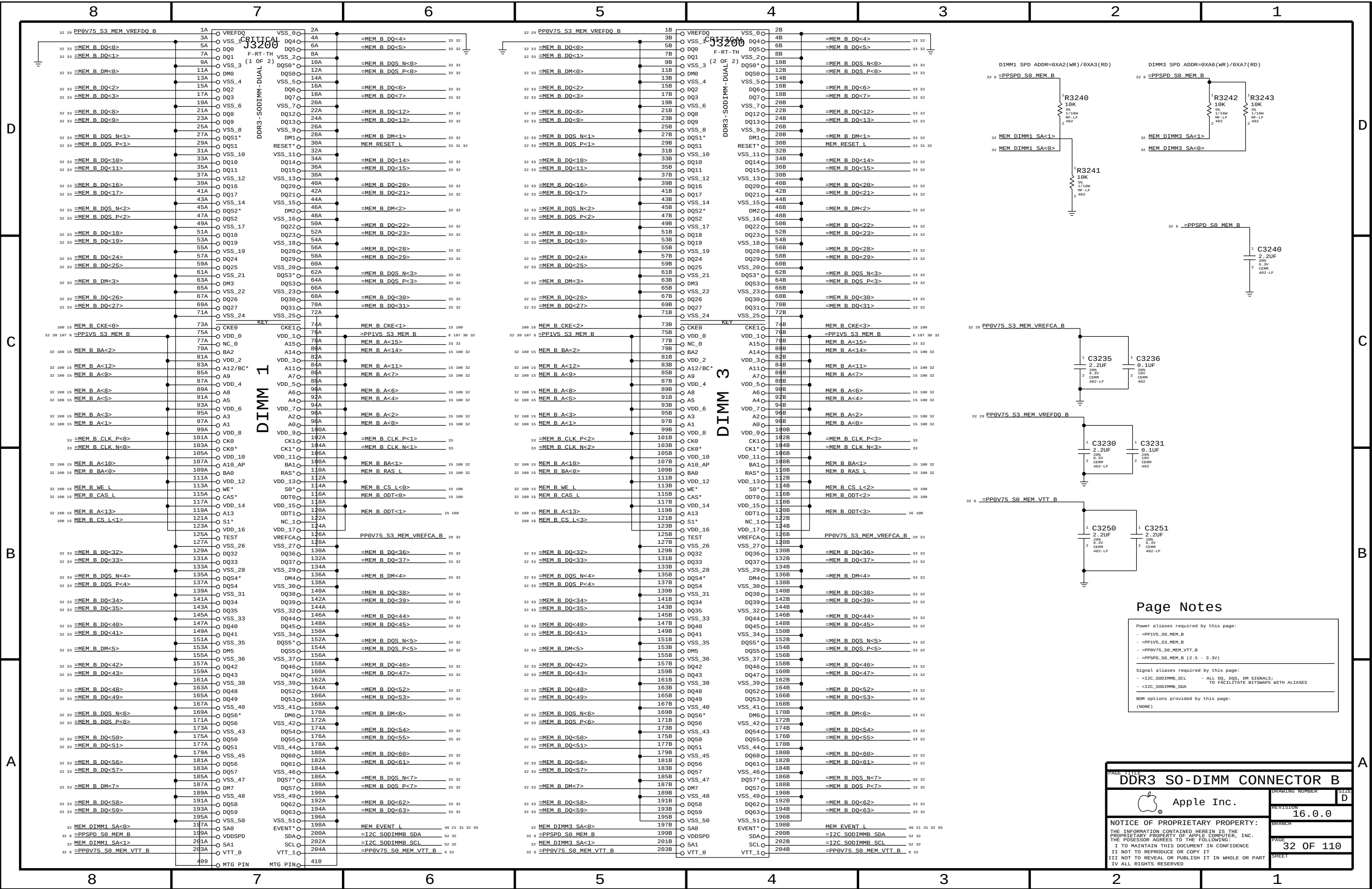
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Page Notes

Power aliases required by this page:

- PP1V5_S0_MEM_B
- PP1V5_S3_MEM_B
- PP0V75_S0_MEM_VTT_B
- PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:

- I2C_S0DIMMB_SCL - ALL DQ, DQS, DM SIGNALS;
- I2C_S0DIMMB_SDA TO FACILITATE BITSTREAMS WITH ALIASES

BOM options provided by this page:

(NONE)

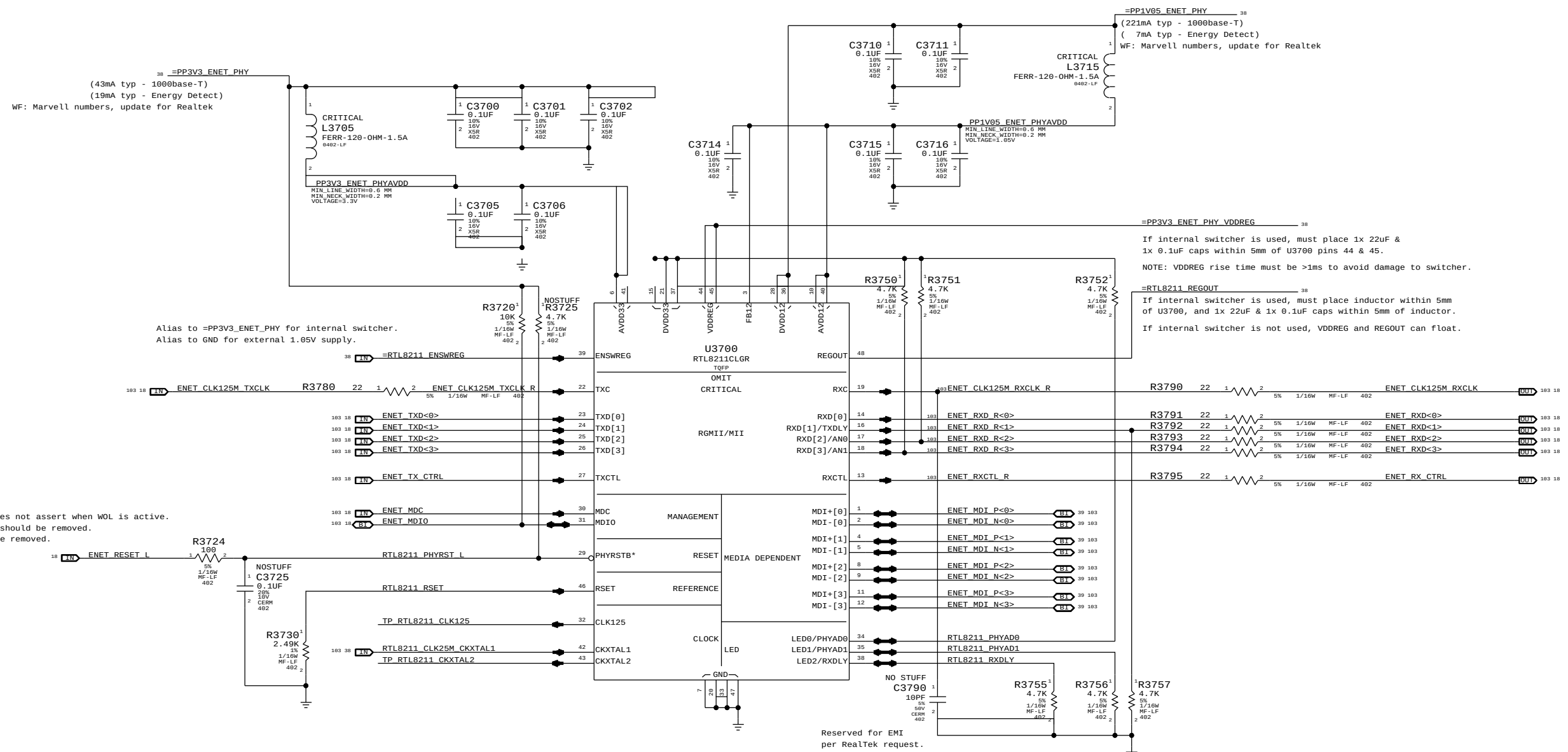
DDR3 SO-DIMM CONNECTOR B

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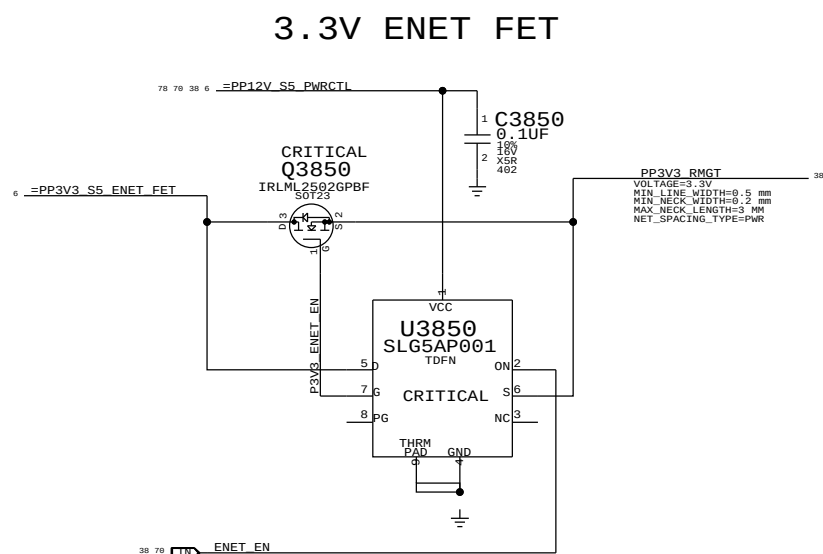
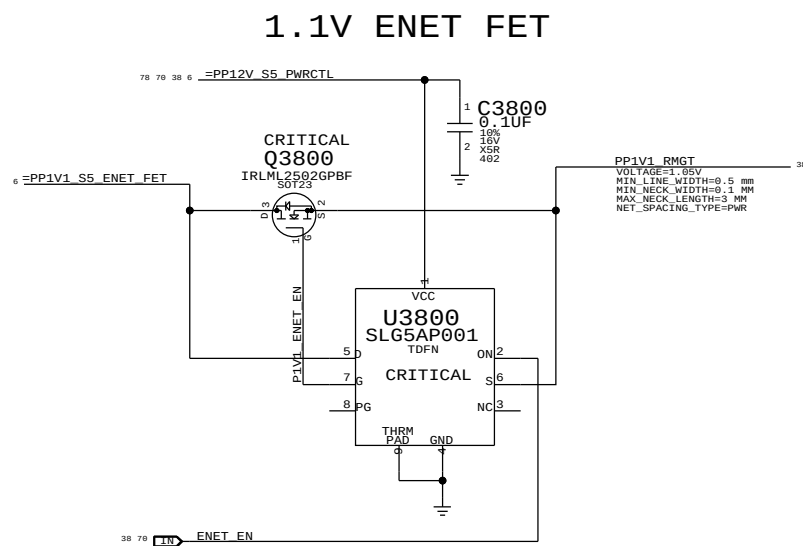
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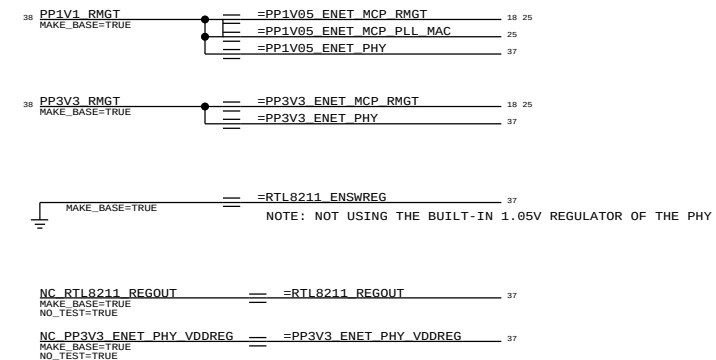


Configuration Settings:

PHYAD	=	01	(PHY Address 00001)
AN[1:0]	=	11	(Full auto-negotiation)
RXDLY	=	0	(RXCLK transitions with data)
TXDLY	=	0	(No TXCLK Delay)

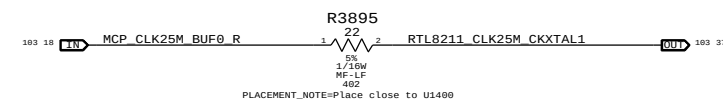


ENET ALIASES

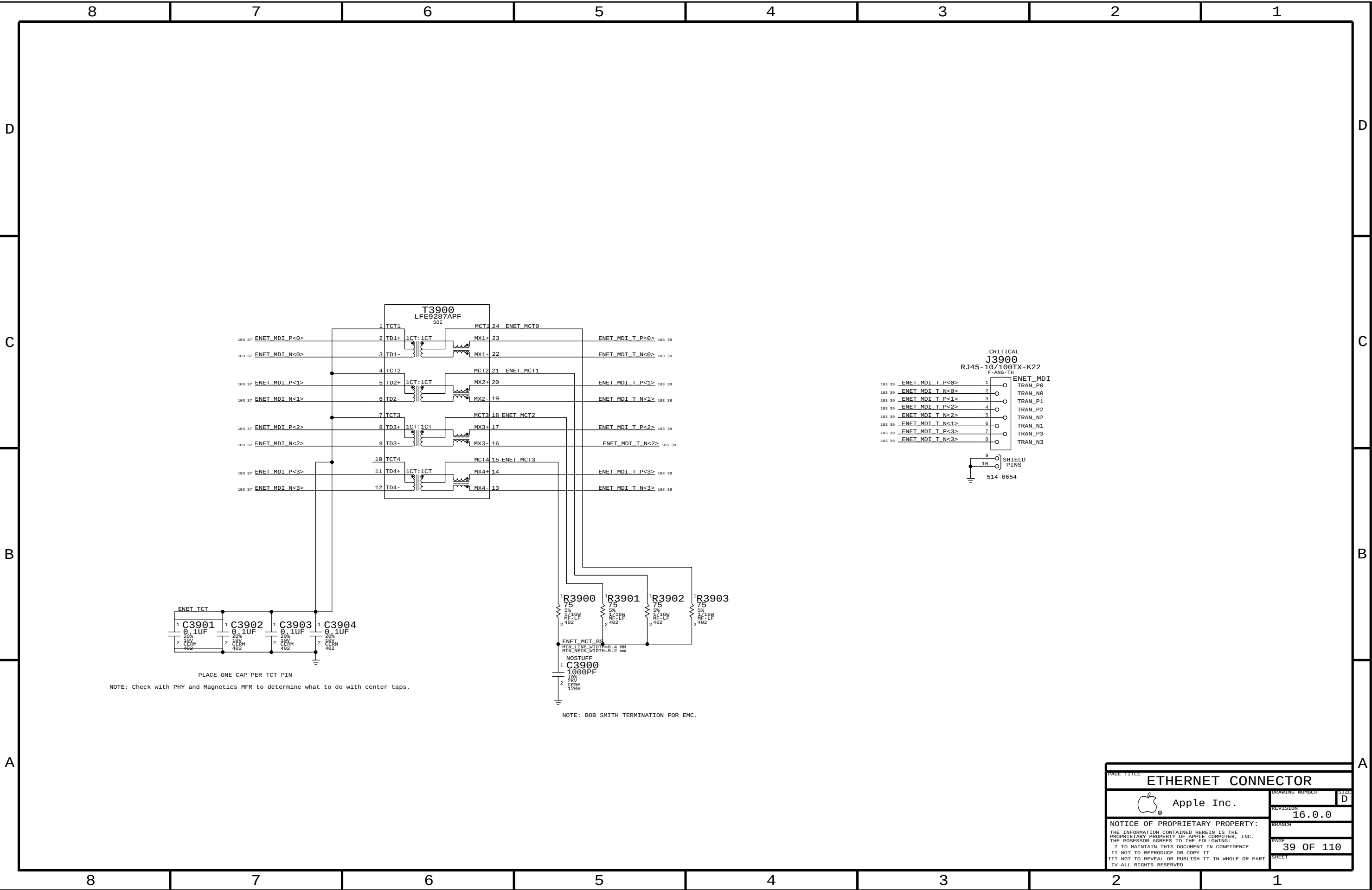


RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered. Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



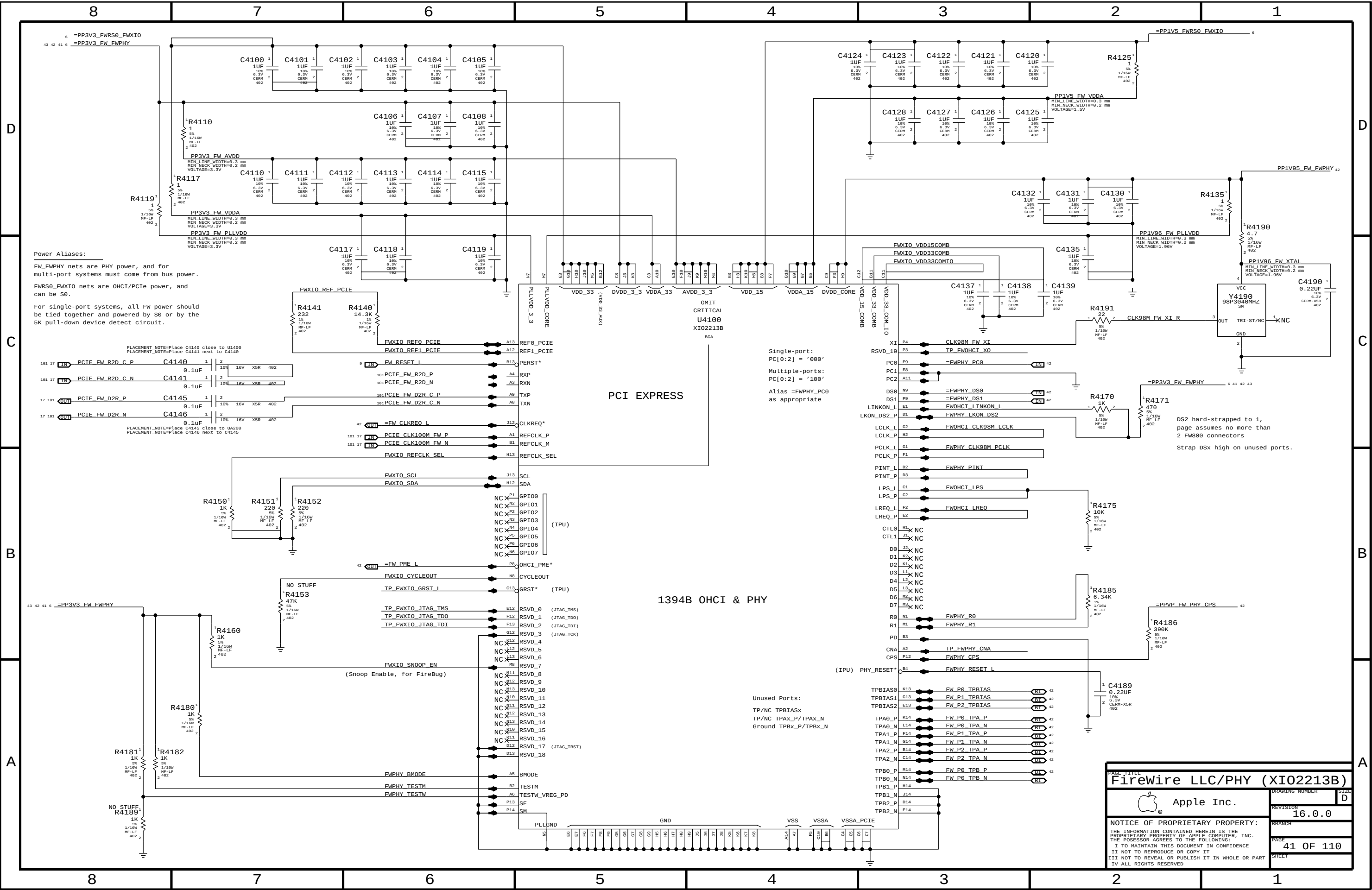
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FireWire LLC/PHY (XI02213B)

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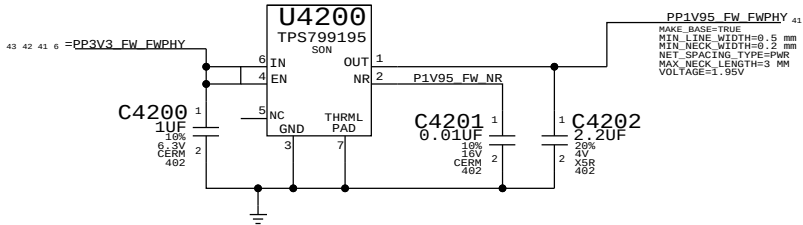
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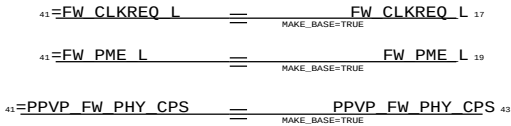
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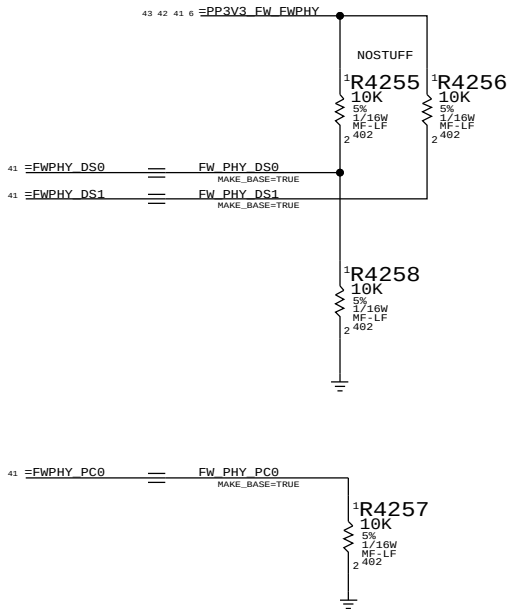
1394 PHY 1.95V SUPPLY



FireWire Aliases For Connectivity



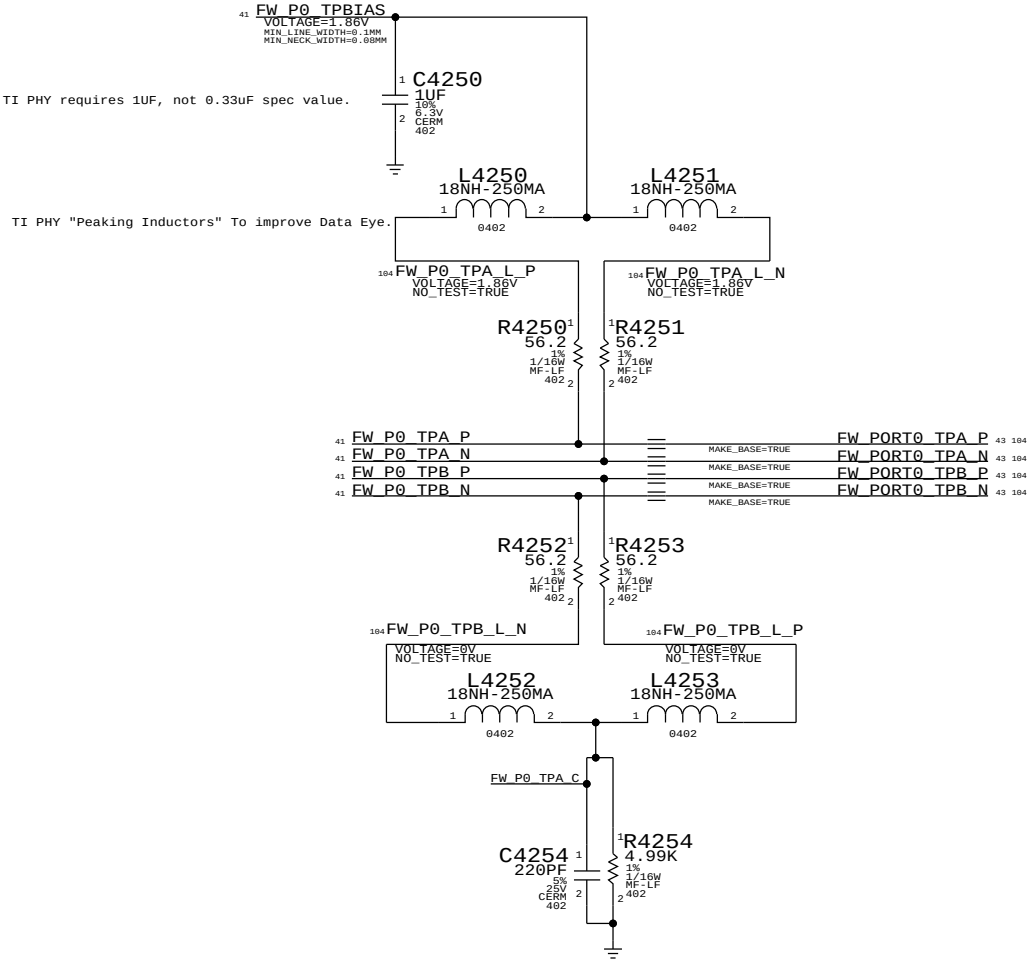
1394 PHY STRAPPING OPTIONS



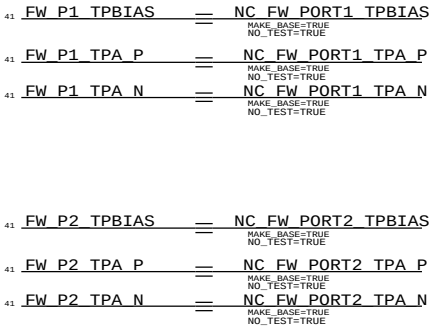
THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE.

iMacs are now one port only and have Power Code "000"

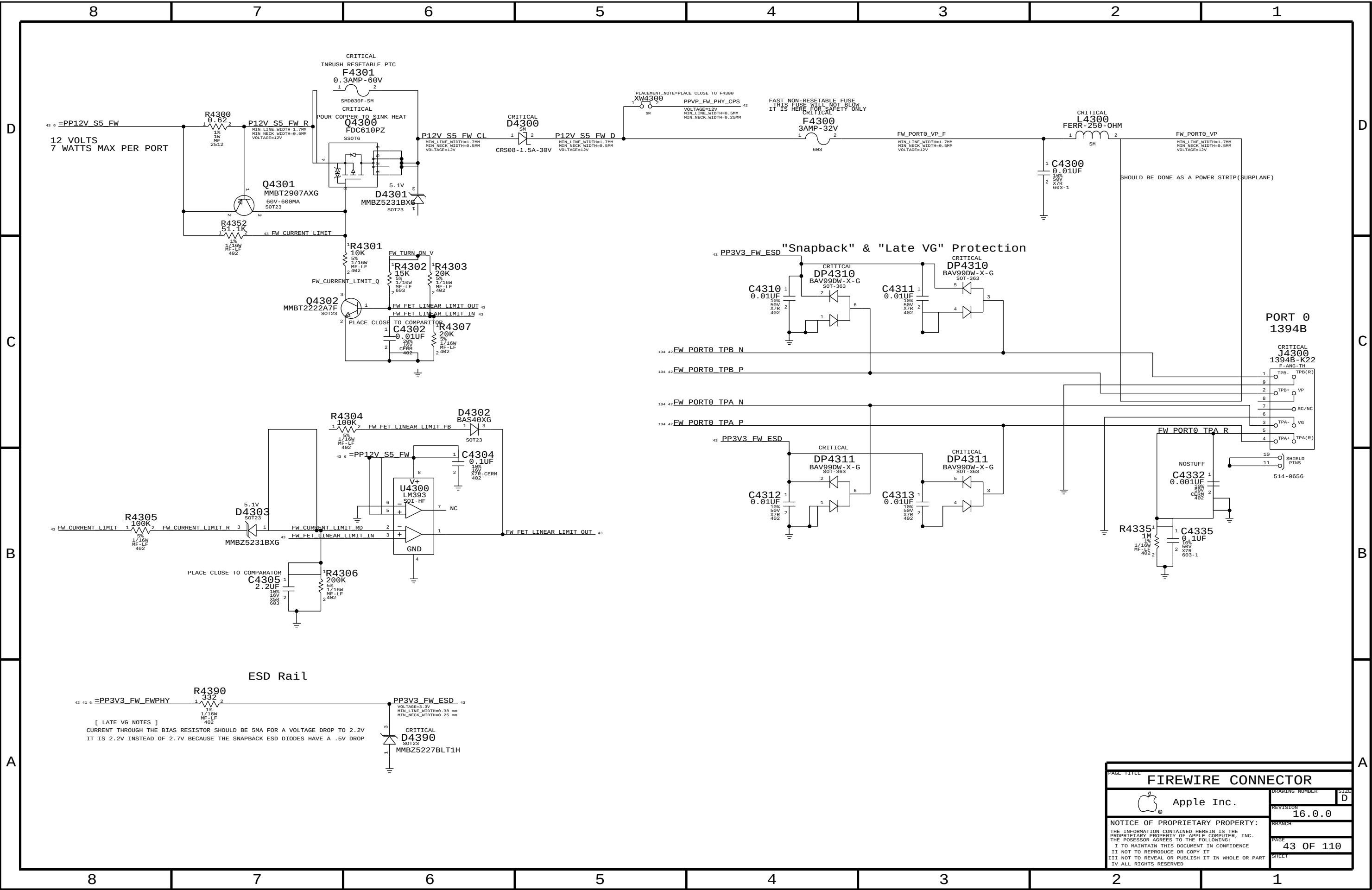
Termination
Place close to FireWire PHY



2ND & 3RD TPA/TPB PAIR UNUSED



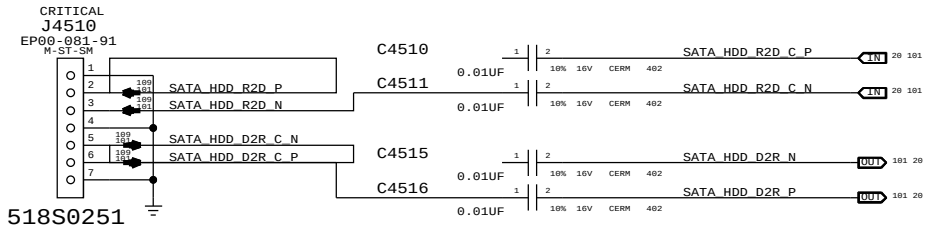
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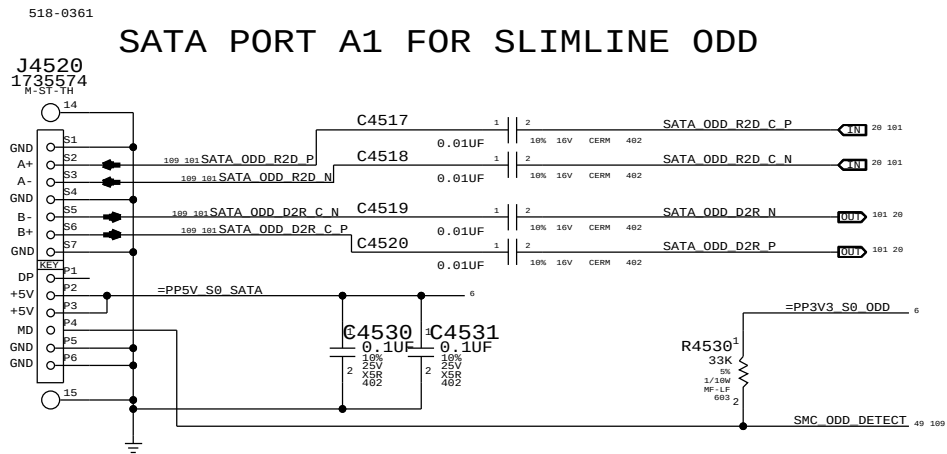
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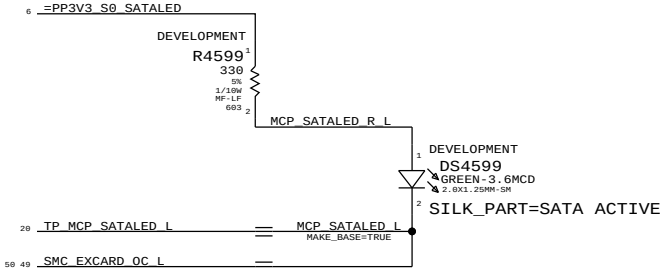
SATA PORT A0 FOR HDD

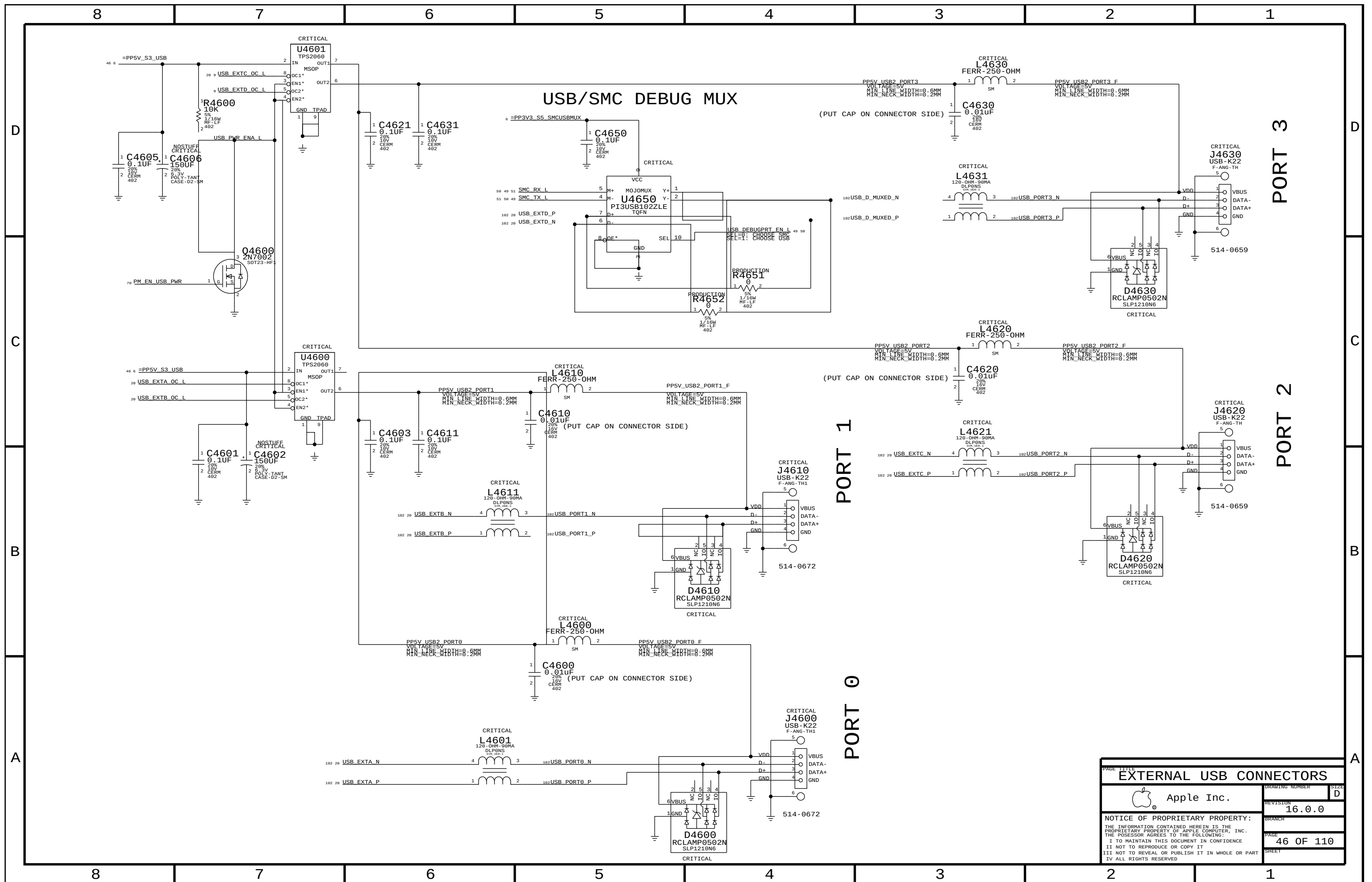


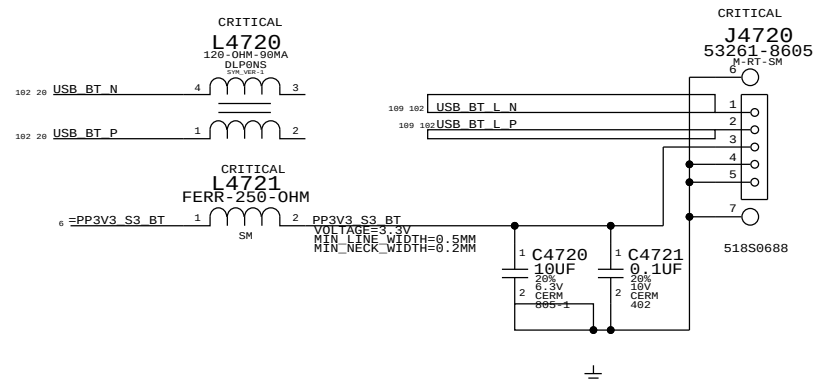
SATA PORT A1 FOR SLIMLINE ODD



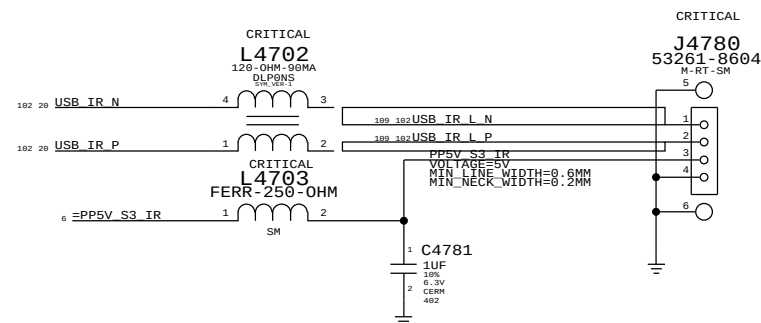
SATA Activity LED



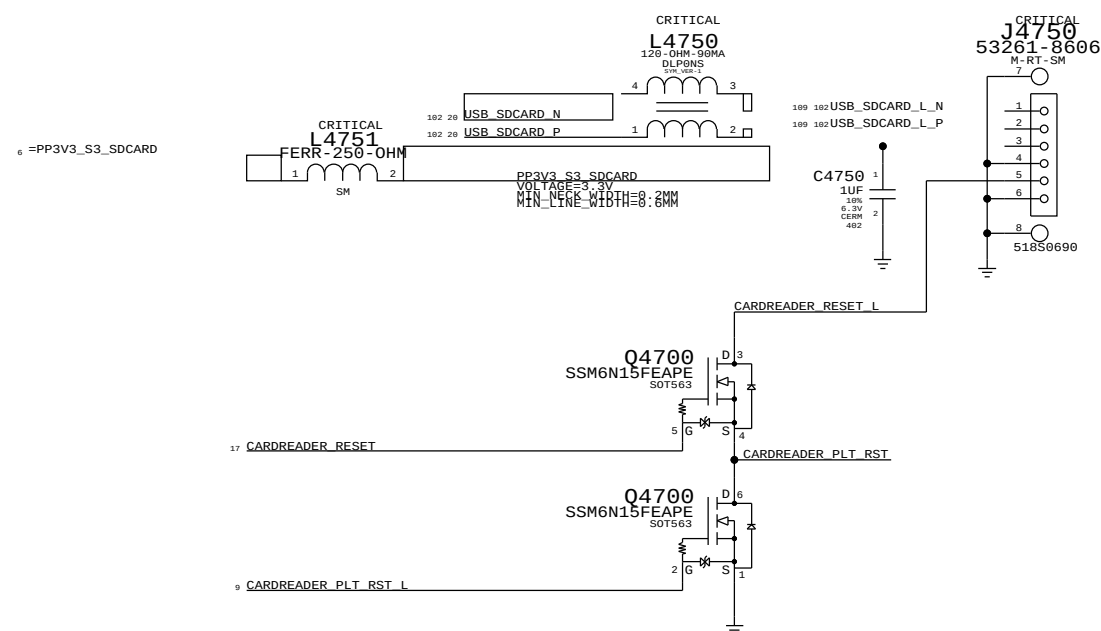


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IR RECEIVER CONNECTOR

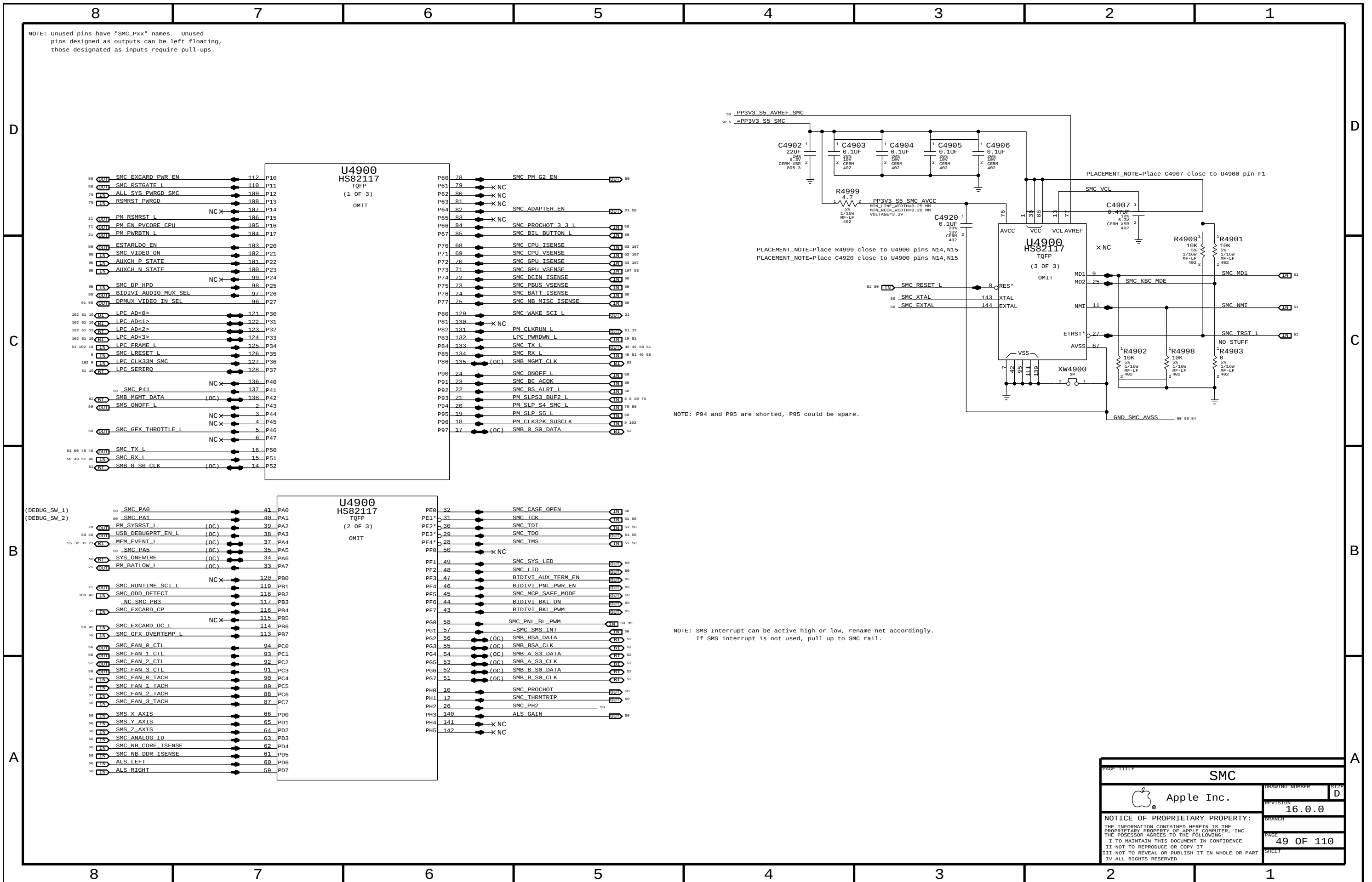


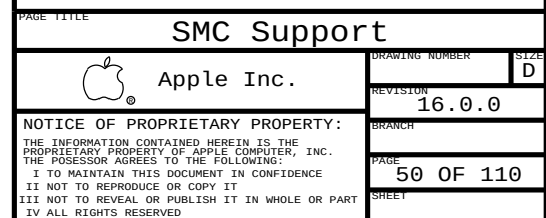
SD Card Reader Board Connector

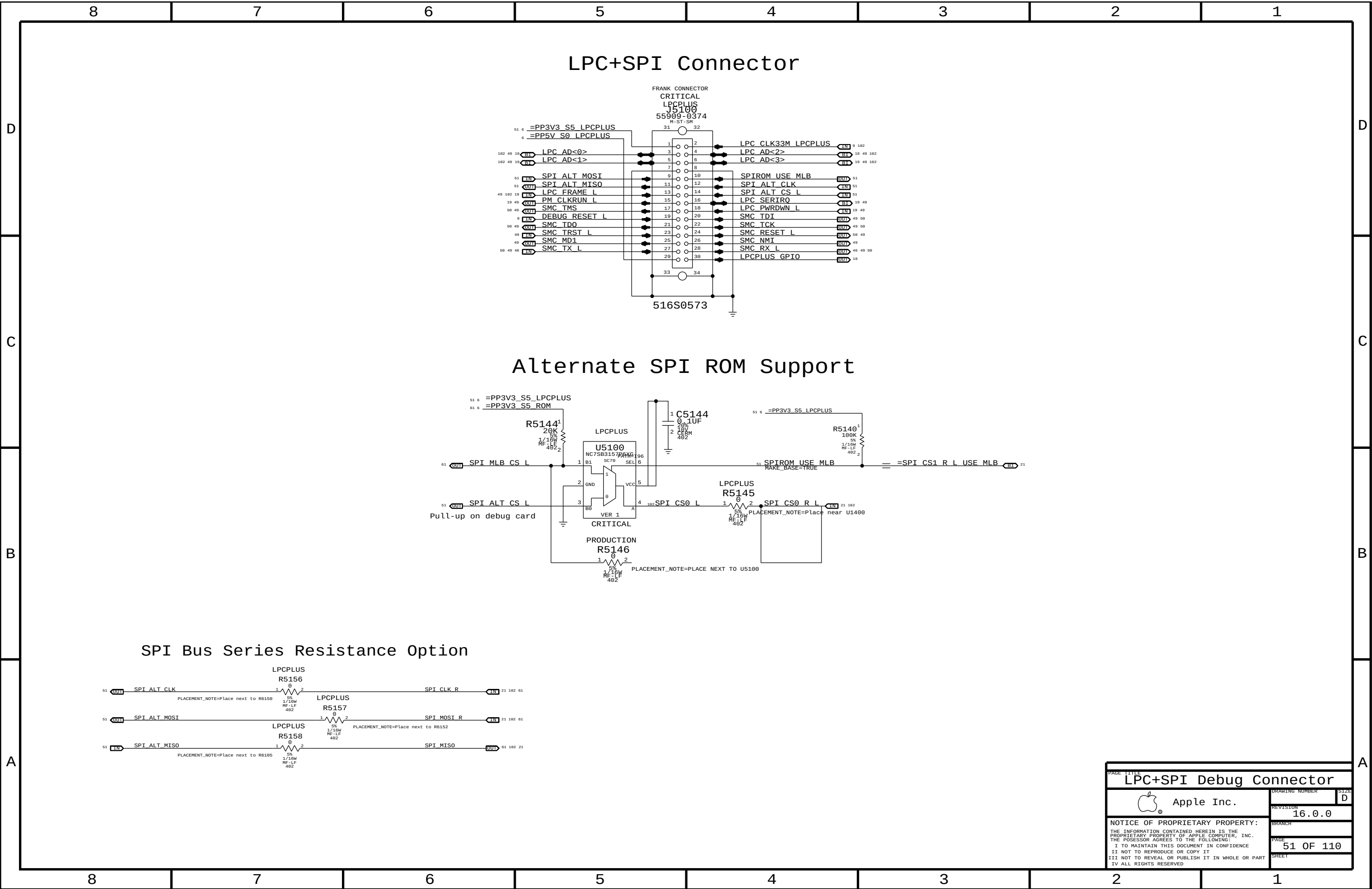


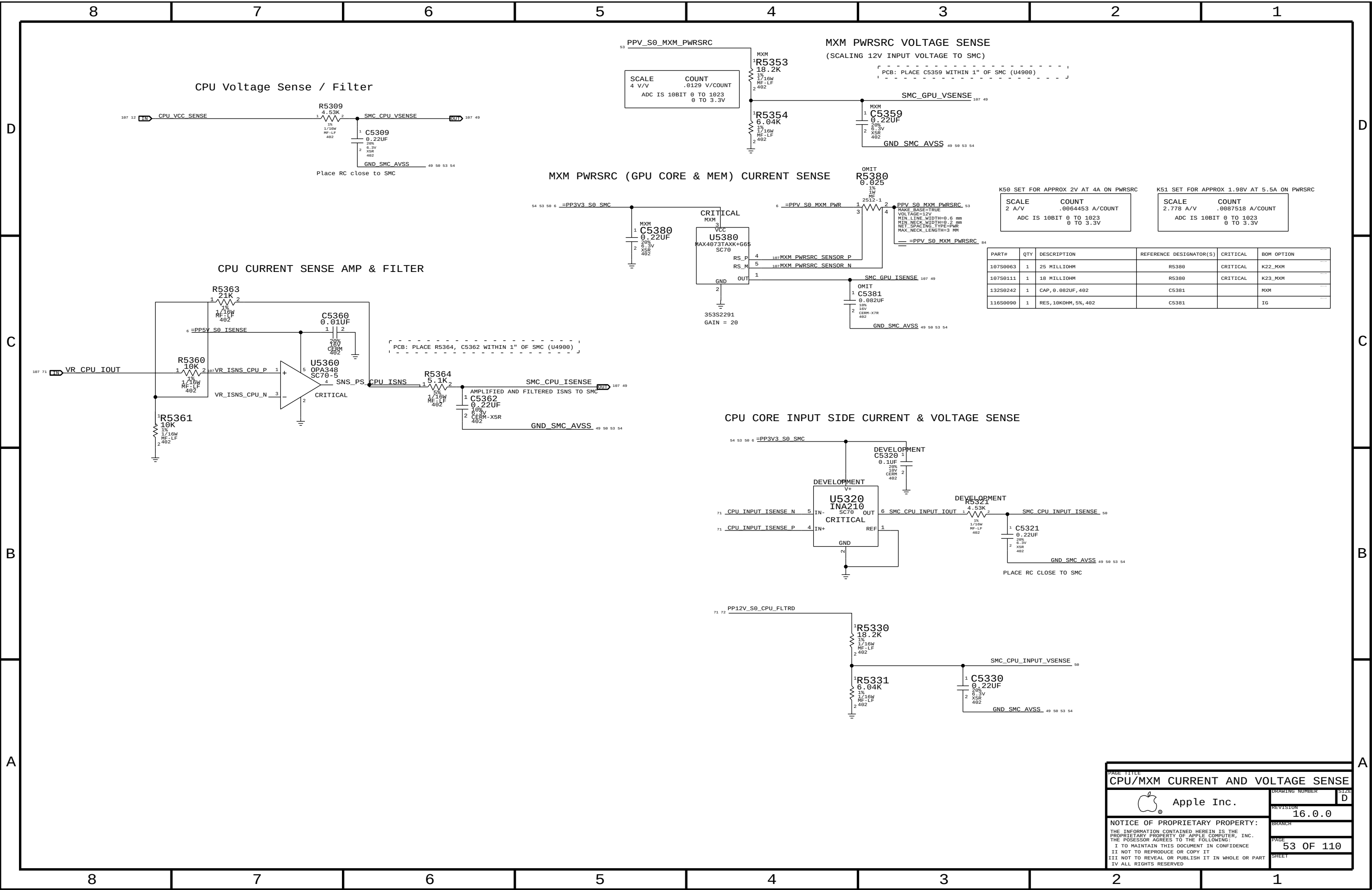
PAGE TITLE		DRAWING NUMBER	
Internal USB Connections		SIZE	
 Apple Inc.		REVISION	
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		BRANCH	
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		SHEET	

[illegible]



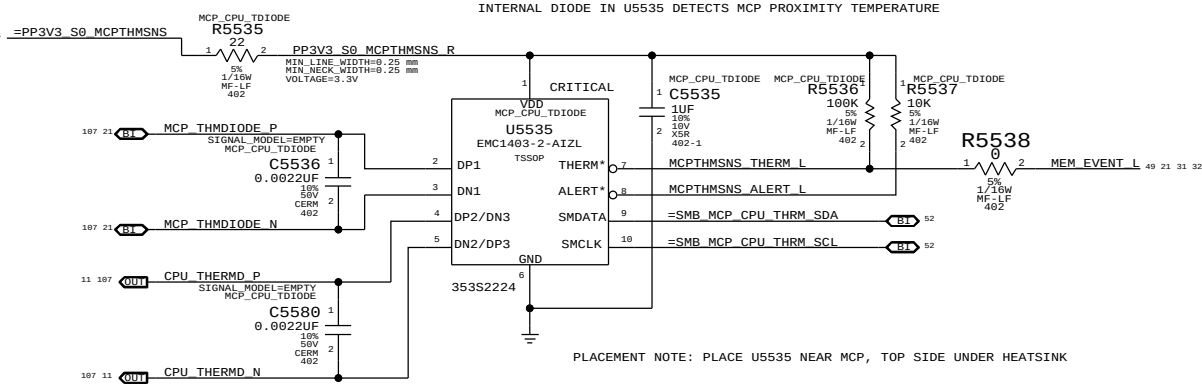




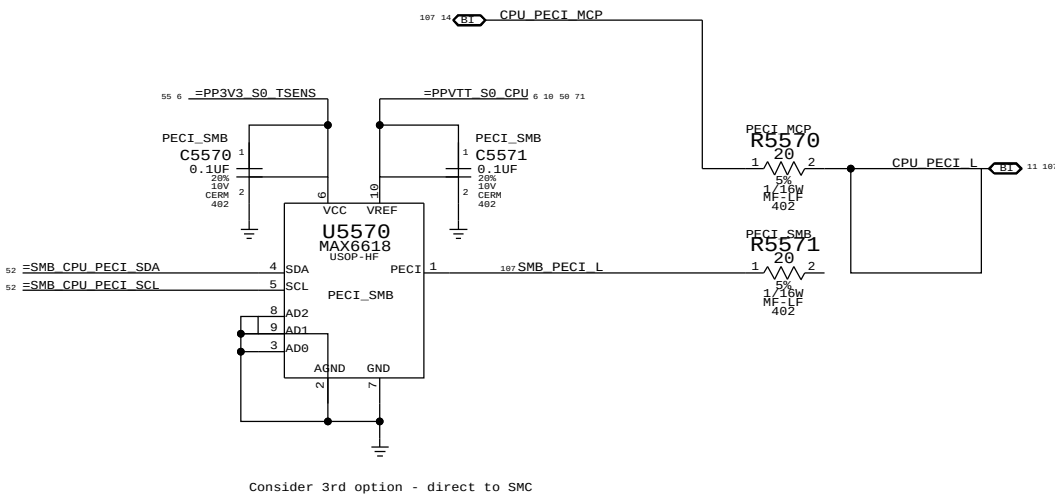


REMOTE THERMAL SENSORS
HEATSINKS, AMBIENT, PANEL AND ODD

MCP & CPU T-Diode Thermal Sensor



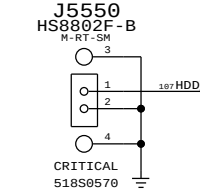
CPU PECCI DTS OPTIONS



REMOTE THERMAL SENSORS (HEATSINKS AND ODD)

HDD OUT OF BAND TEMPERATURE SENSING LEVEL SHIFTING

SILK_PART=HDD TEMP

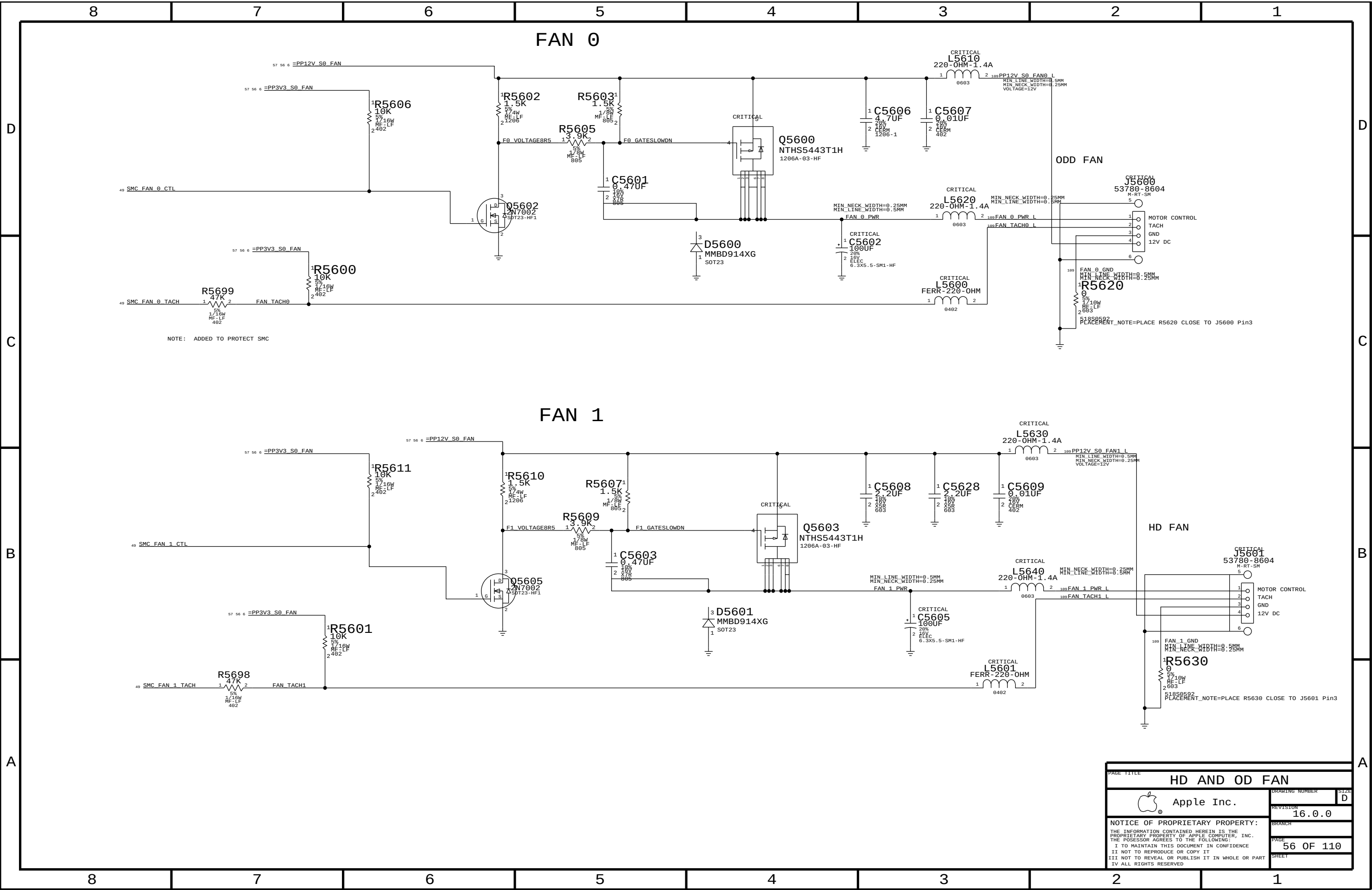


Drive active = valid signal, HDD OOB TEMP low
Drive disconnected = pulled high

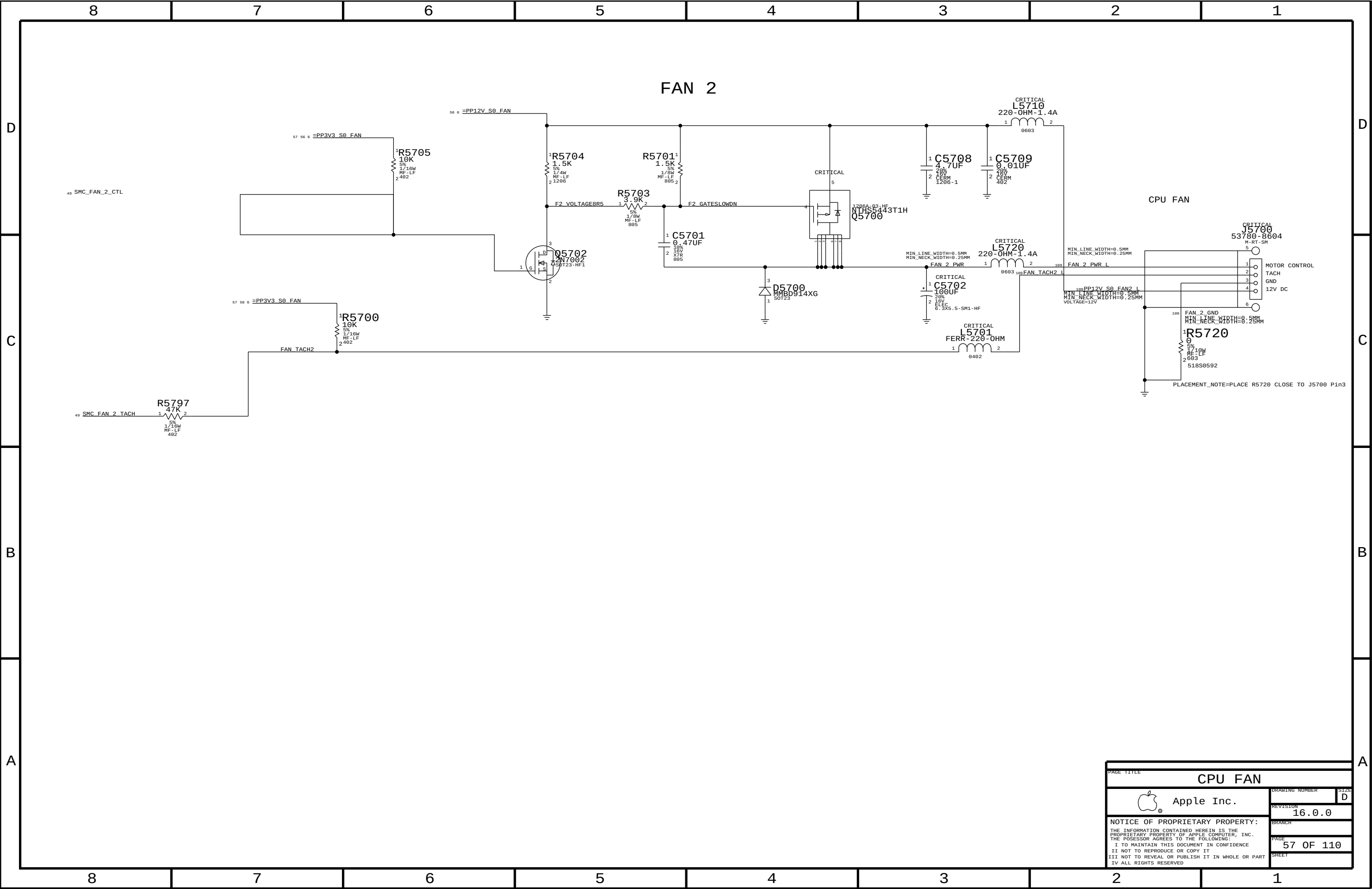
Cannot pull low because some drives use this bit to determine 1.5 Gbps vs. 3.0 Gbps SATA

Must pull high to 2.5V for compatibility with all drives

Thermal Sensors	
Apple Inc.	REVISION 16.0.0
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PAGE TITLE			
HD AND OD FAN			
 Apple Inc.	DRAWING NUMBER		SIZE
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	BRANCH		
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CPU FAN		
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8	7	6	5	4	3	2	1		
D									D
C									C
B									B
A									A
8	7	6	5	4	3	2	1		

PAGE TITLE

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SIZE

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D

C

B

A

D

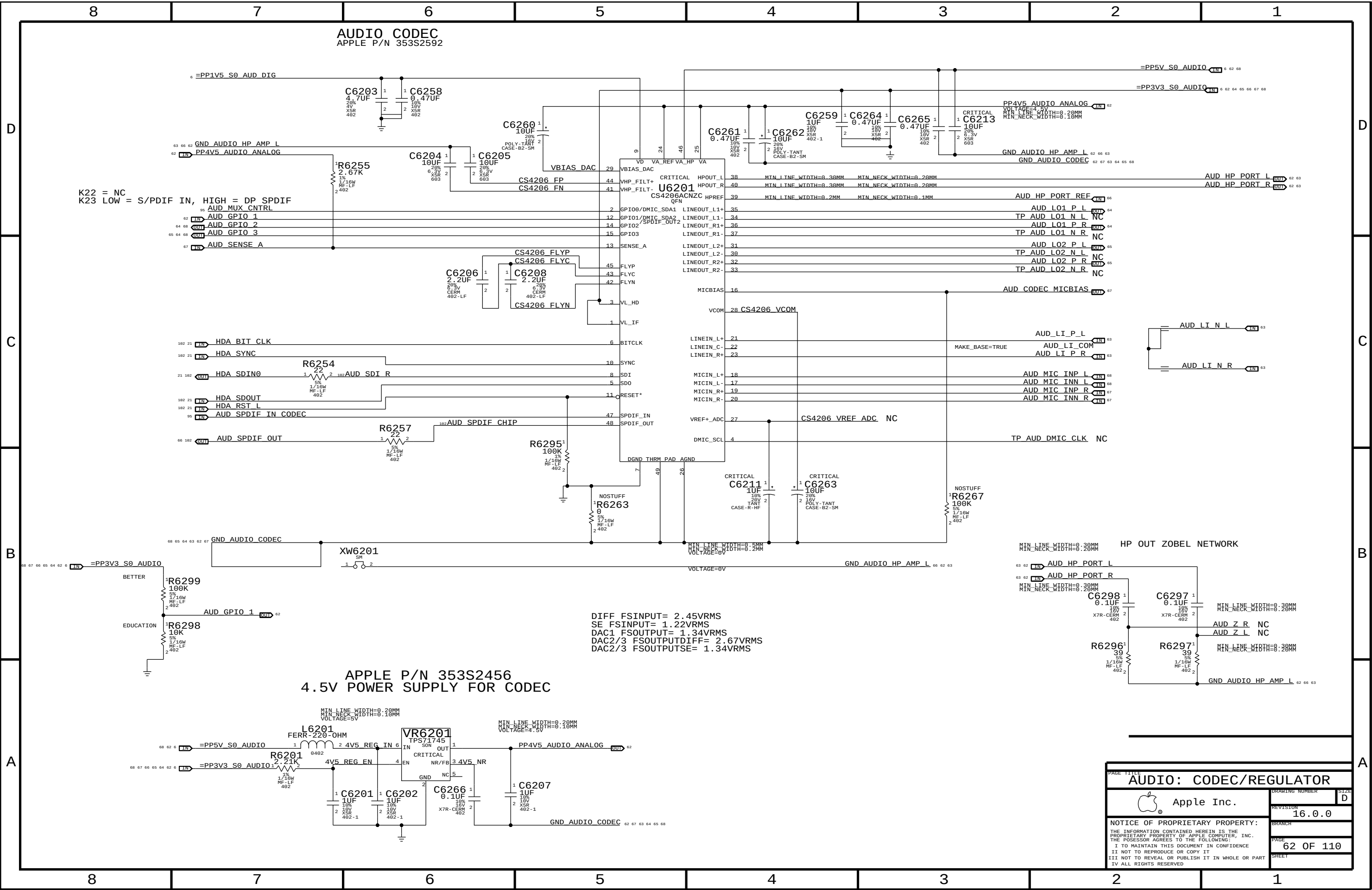
C

B

A

	8	7	6	5	4	3	2	1	
D									D
C									C
B									B
A									A
	8	7	6	5	4	3	2	1	

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		PAGE 60 OF 110	SHEET



MIN LINE WIDTH=0.3MM
MIN NECK WIDTH=0.3MM

R6324
0
5%
1/10W
MF-LF
693

AUD_HP_PORT L

62

66

AUD_HP_L

NOSTUFF
CRITICAL

C6320
1
2209PF
50V
CBG-CERM
693

62

GND_AUDIO_HP_AMP L

66

NOSTUFF
CRITICAL

C6321
1
2209PF
50V
CBG-CERM
693

62

AUD_HP_PORT R

62

66

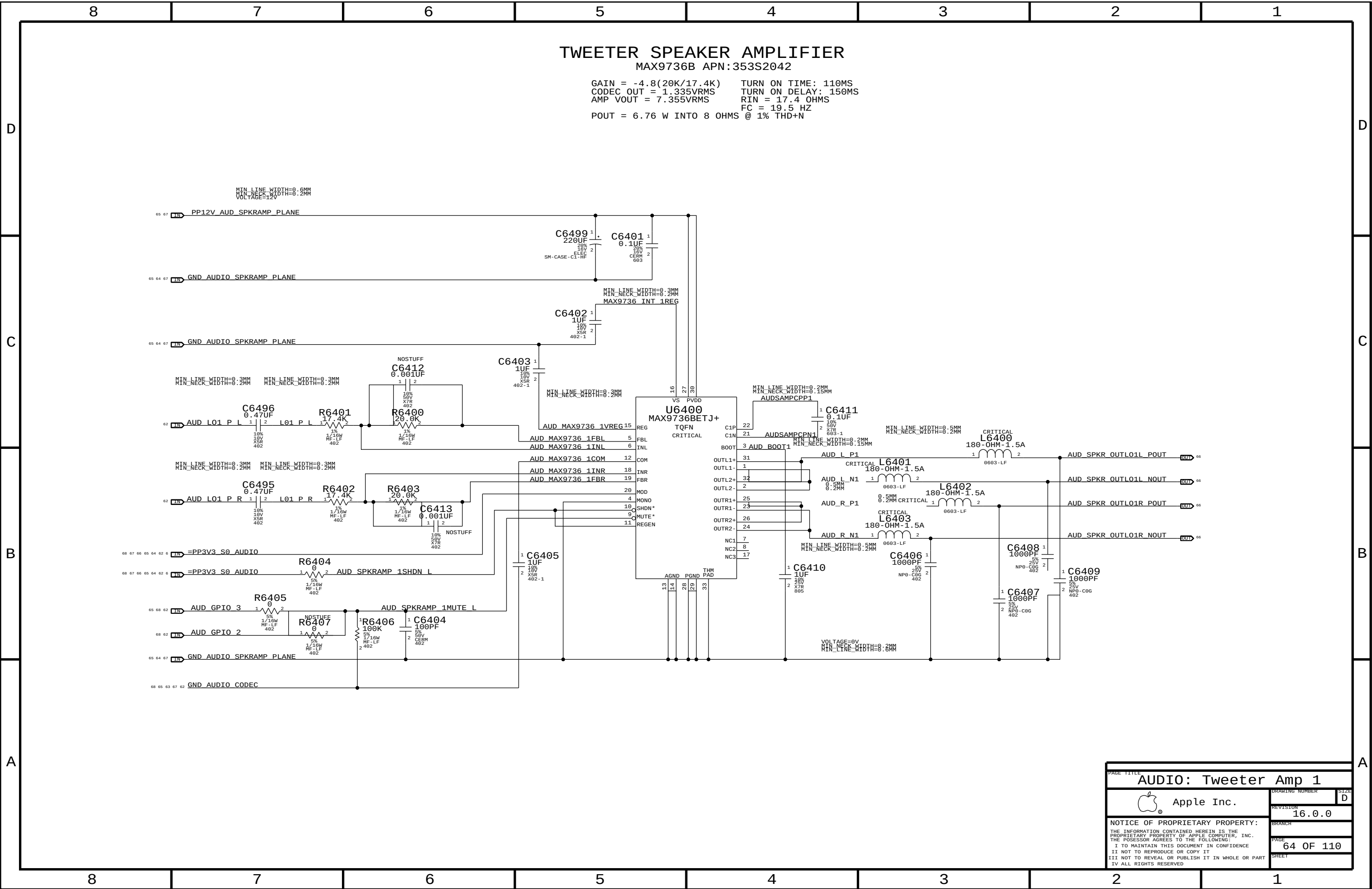
AUD_HP_R

R6325
0
5%
1/10W
MF-LF
693

MIN LINE WIDTH=0.3MM
MIN NECK WIDTH=0.3MM

PCB layout for the audio CODEC section, showing four channels (L, R, L, R) with components like resistors (R6300, R6301, R6302, R6303, R6304, R6305), capacitors (C6301, C6302, C6303, C6304, C6305), and critical components (C6300, C6301, C6302, C6303, C6304, C6305). The layout includes labels for MIN_NECK_WIDTH=0.2MM and MIN_LINE_WIDTH=0.3MM.

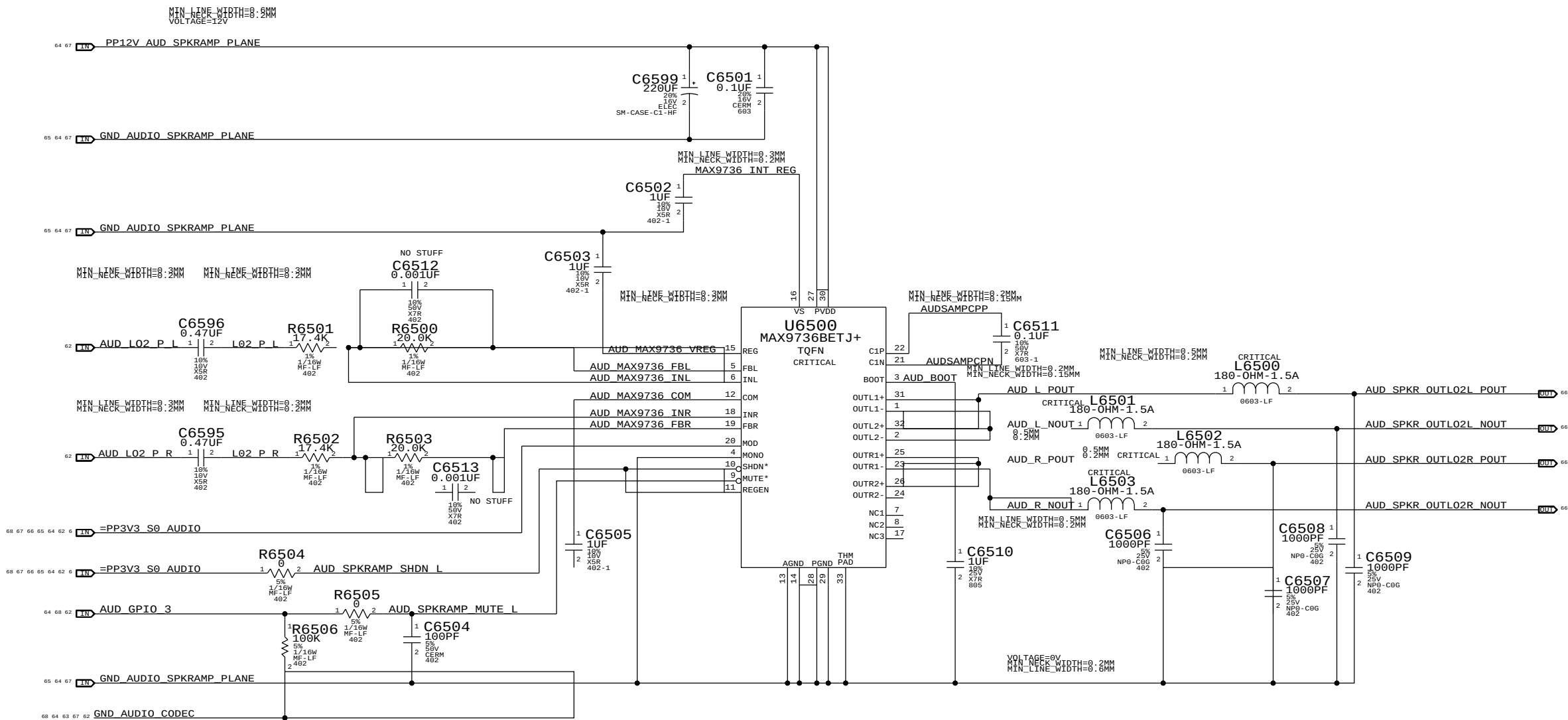
PAGE TITLE		DRAWING NUMBER		SIZE
AUDIO: FILTER/BUFFER				D
 Apple Inc.		REVISION		
		16.0.0		
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		PAGE		
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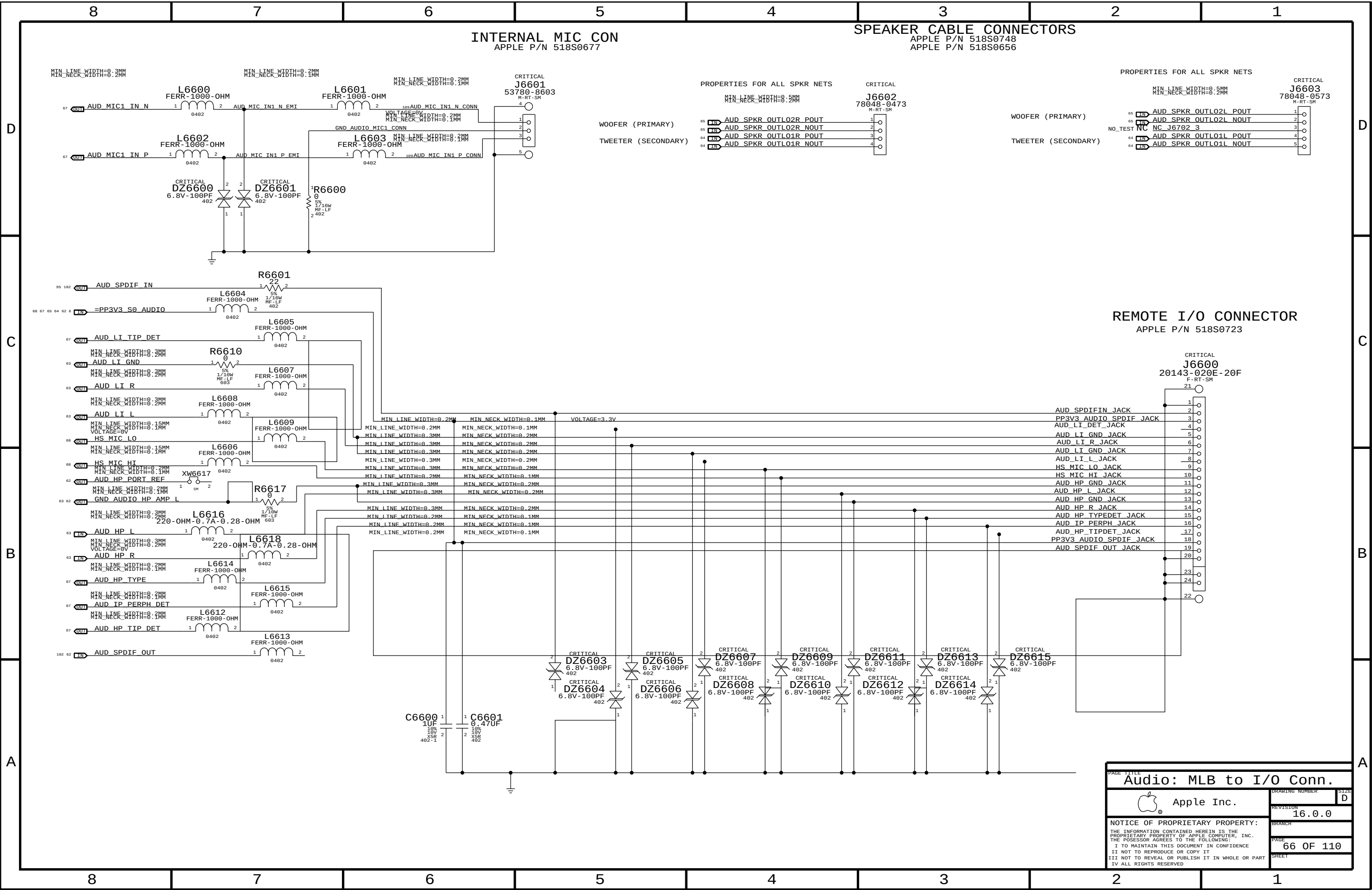
PAGE TITLE		AUDIO: Tweeter Amp 1	
Apple Inc.		DRAWING NUMBER	SIZE
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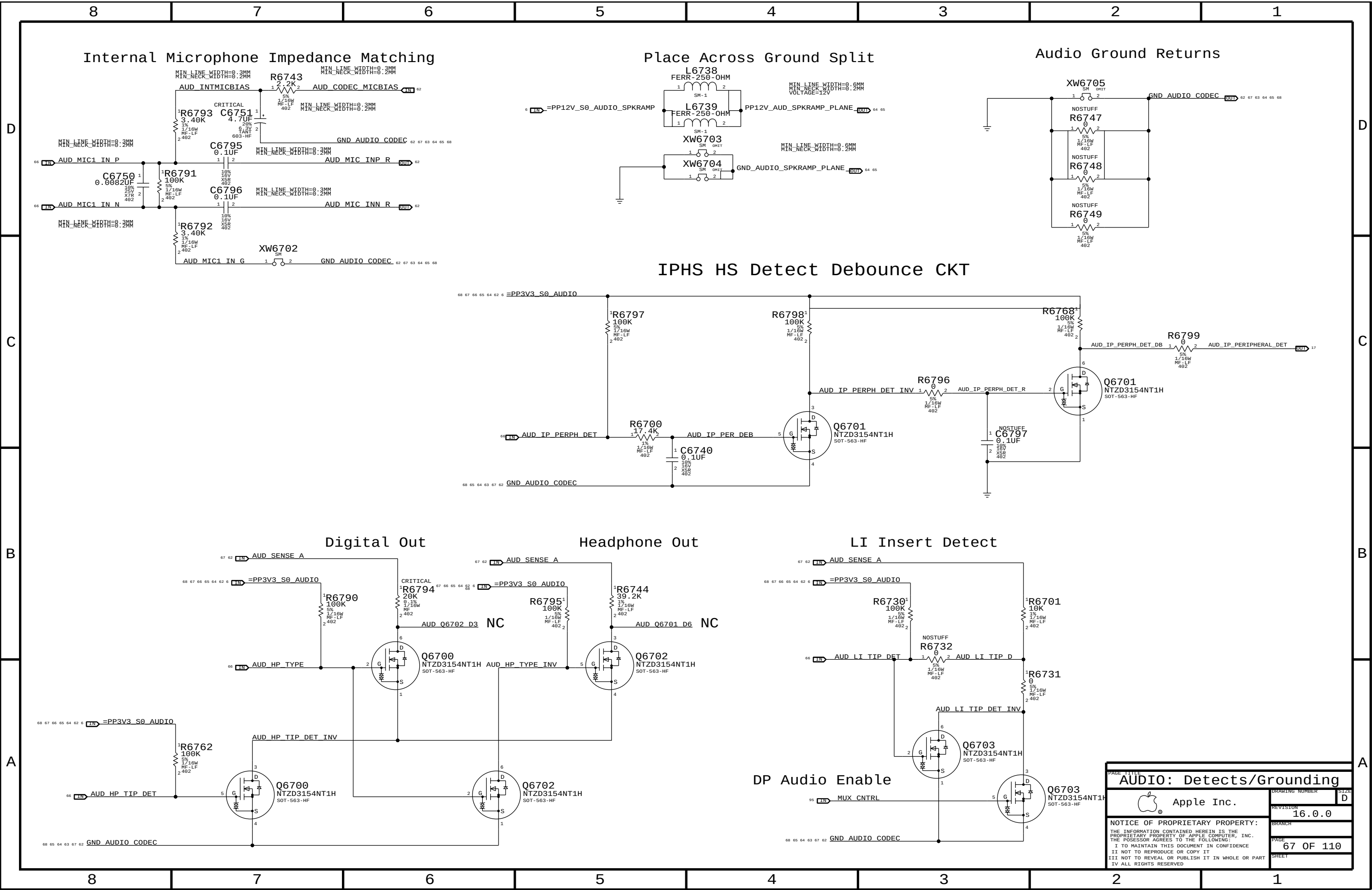
WOOFER SPEAKER AMPLIFIER
MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K) TURN ON TIME: 110MS
CODEC OUT = 1.335VRMS TURN ON DELAY: 150MS
AMP VOUT = 7.355VRMS RIN = 17.4 OHMS
POUT = 6.76 W INTO 8 OHMS @ 1% THD+N FC = 19.5 HZ



PAGE TITLE		AUDIO: Woofer Amp	
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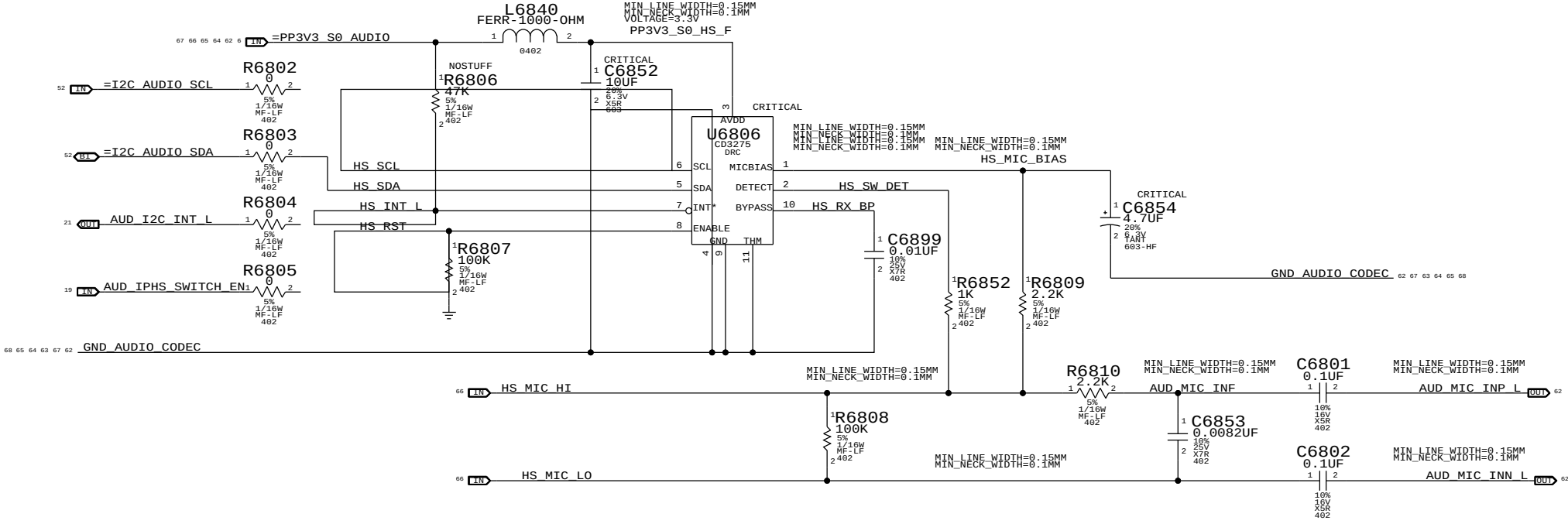




FUNCTION	PIN	CONVERTER	VOLUME	ENABLE/ CNTRL TYPE	DETECT/INTERRUPT
PRIMARY	0X0B	0X04	0X04	GPIO 3	N/A
SECONDARY	0X0A	0X03	0X03	GPIO 3	N/A
HEADPHONES	0X09	0X02	0X02	N/A	0X09 (A)
LINE INPUT	0X0C	0X05	0X05	N/A	LINE IN
BUILT-IN MICROPHONE	0X0D (13, B, RIGHT)	0X06	0X06	MICBIAS 80%	N/A
HEADSET MICROPHONE	0X0D (13, V22, B, LEFT)	0X06	0X06	MIKEY	MIKEY
SPDIF OUT	0X10	0X08	N/A	N/A	0X0C (B)
SPDIF IN	0X0F	0X07	N/A	N/A	N/A
MIKEY	N/A	N/A	N/A	MCP GPIO_38	MCP GPIO_5

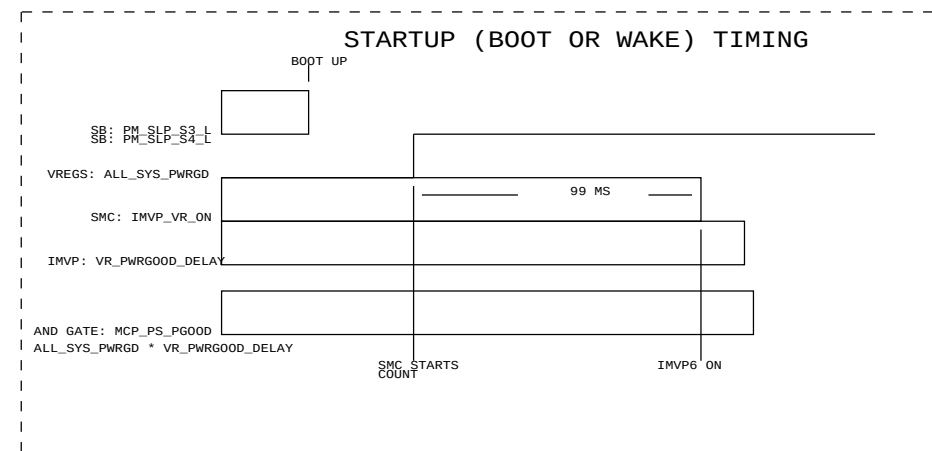
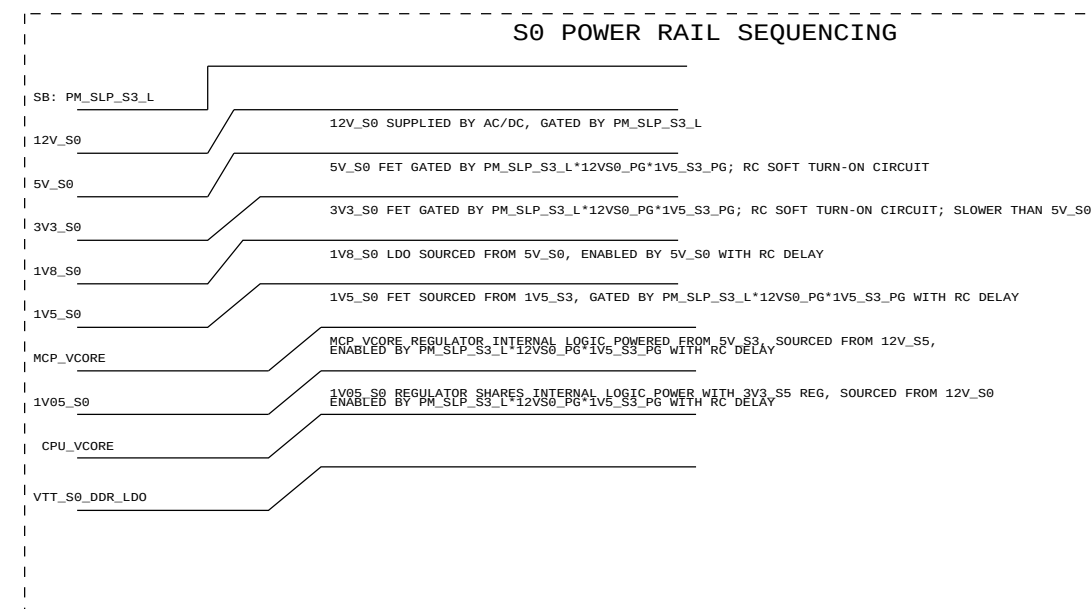
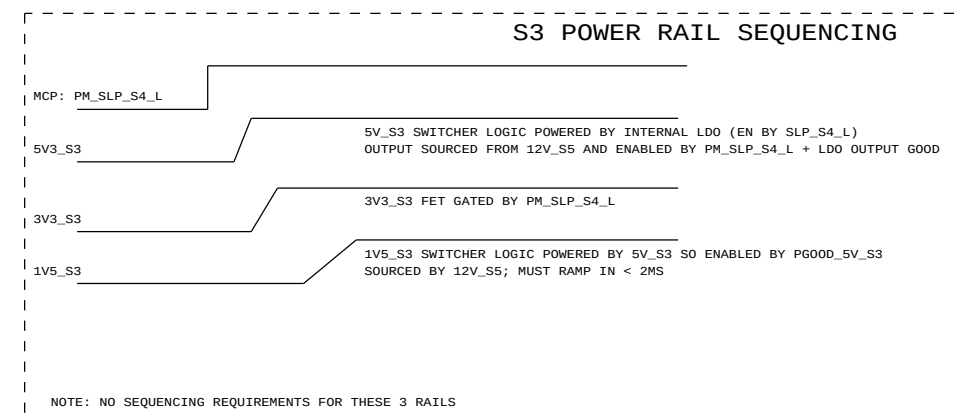
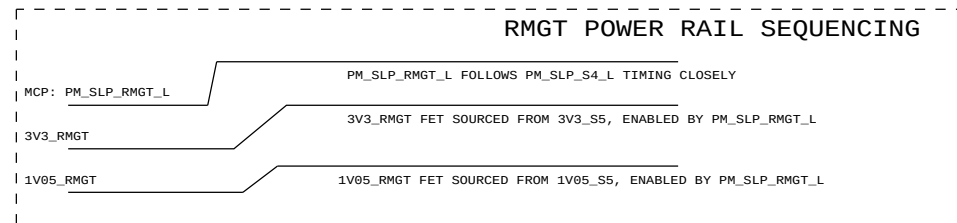
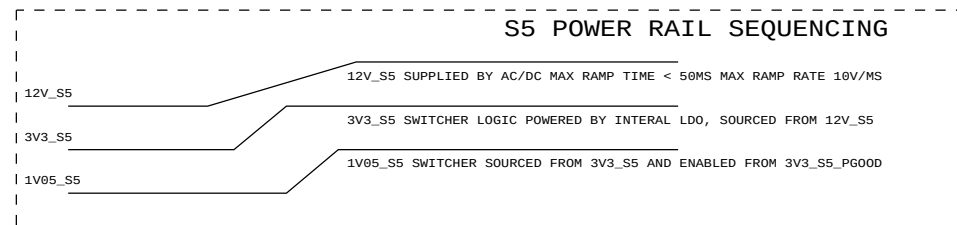
MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2256

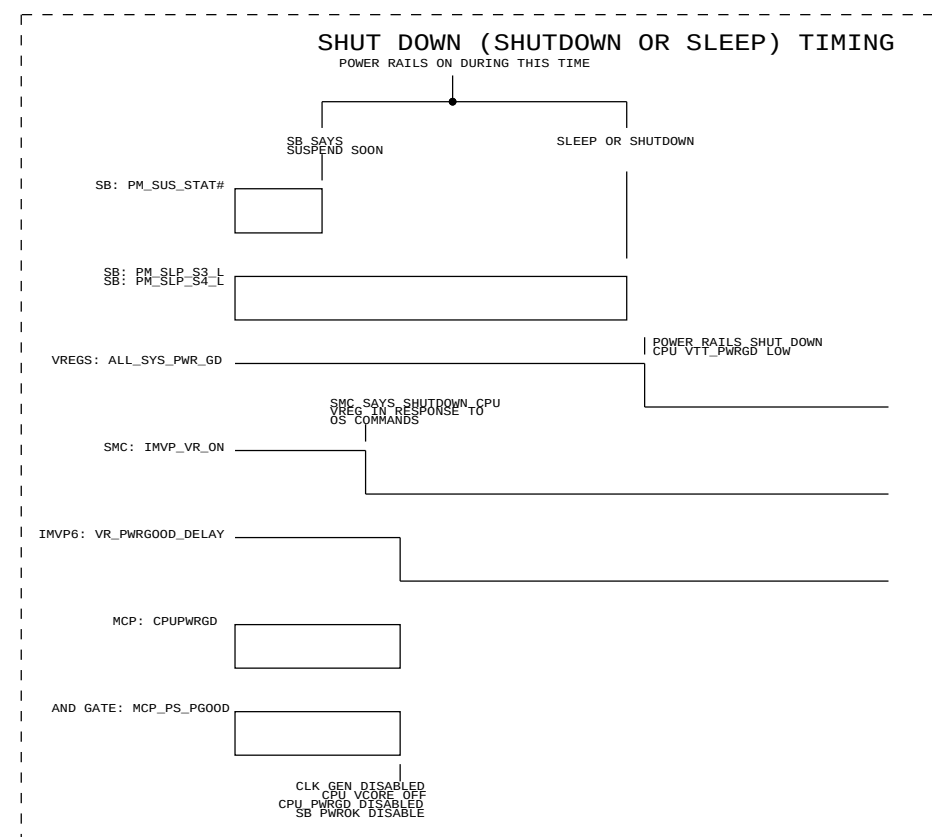


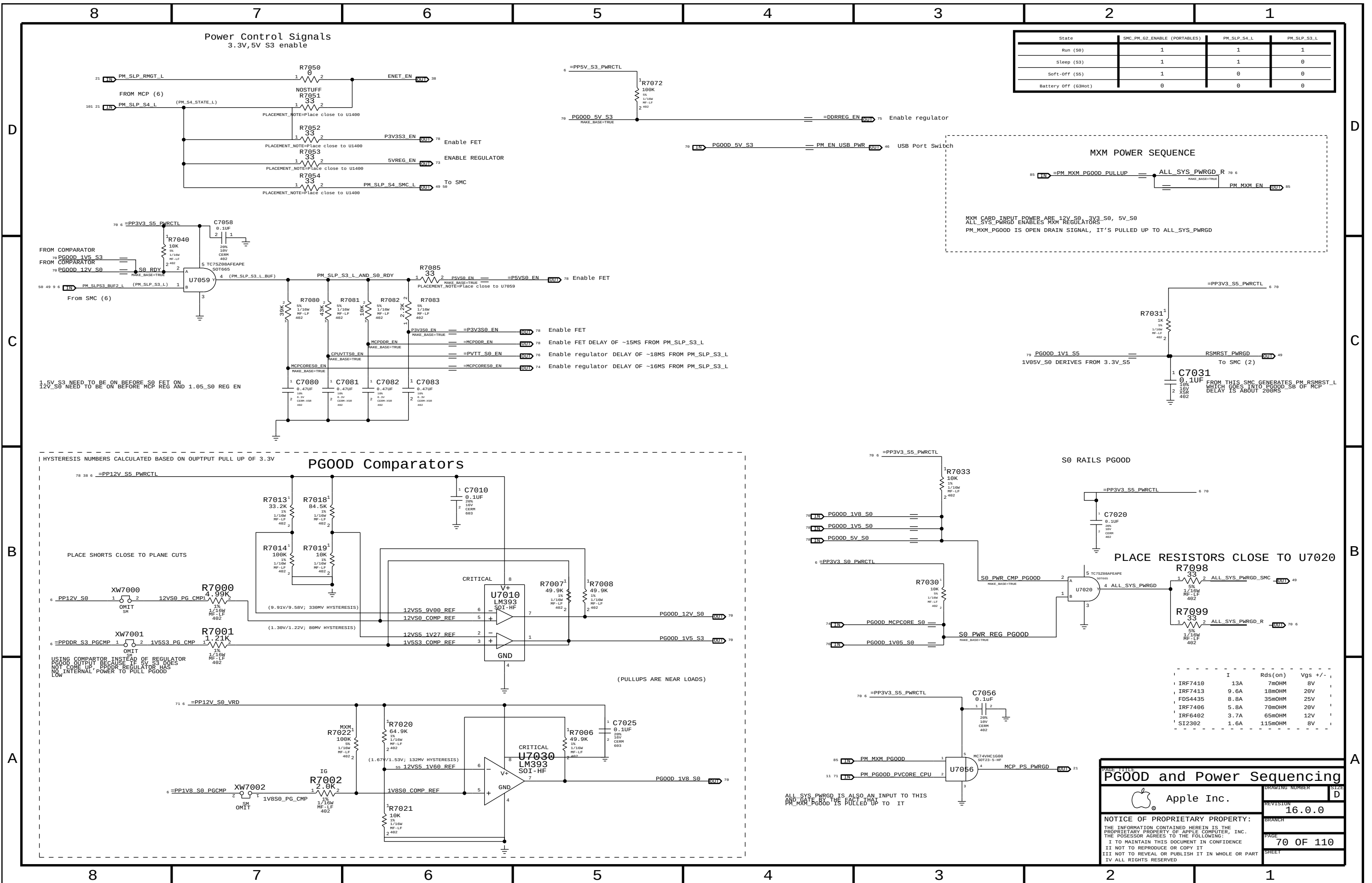
FLP = 8.82 KHZ
FHP = 80 HZ

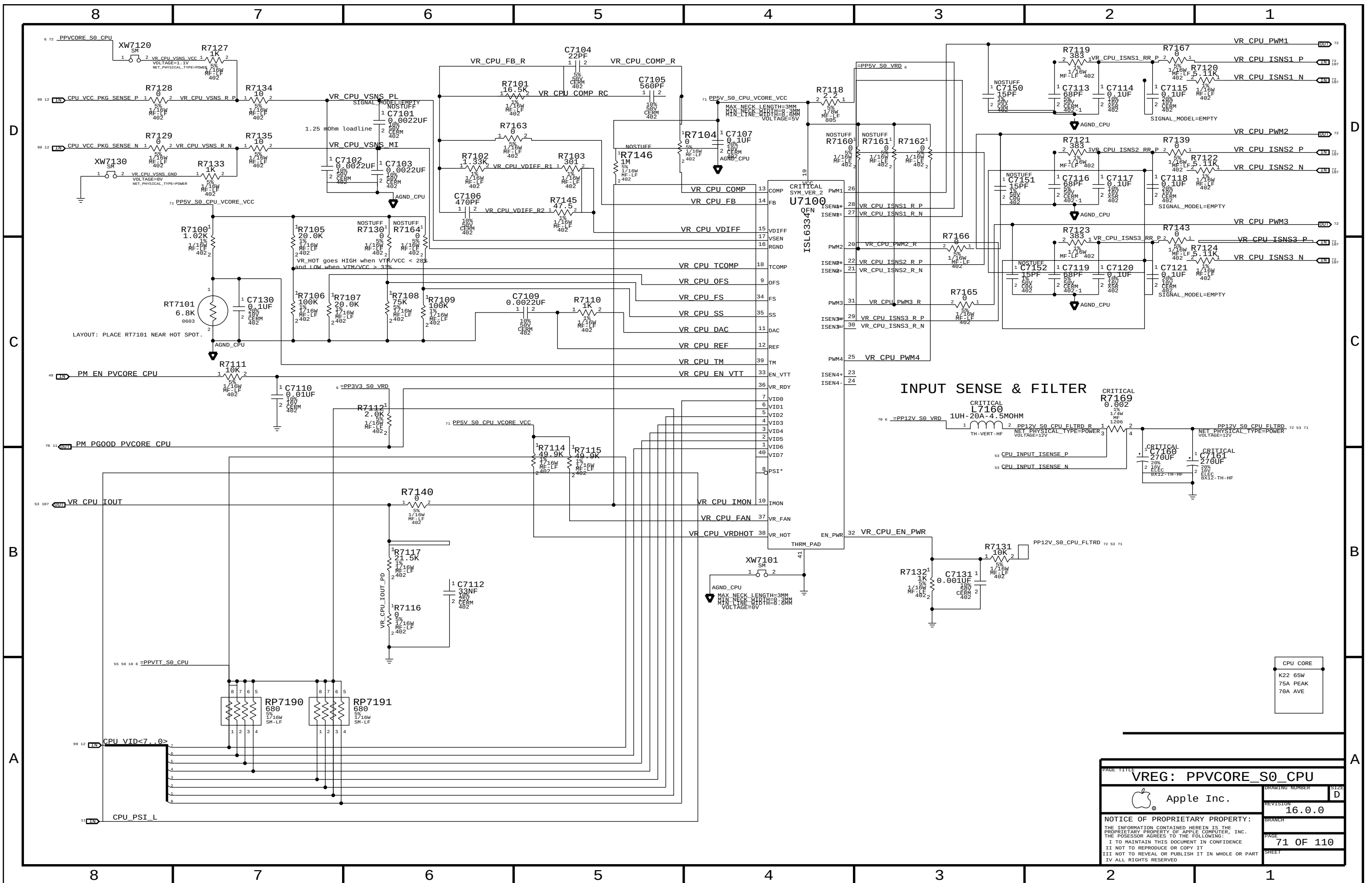
PAGE TITLE		AUDIO: Mikey	
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	16.0.0		SIZE D
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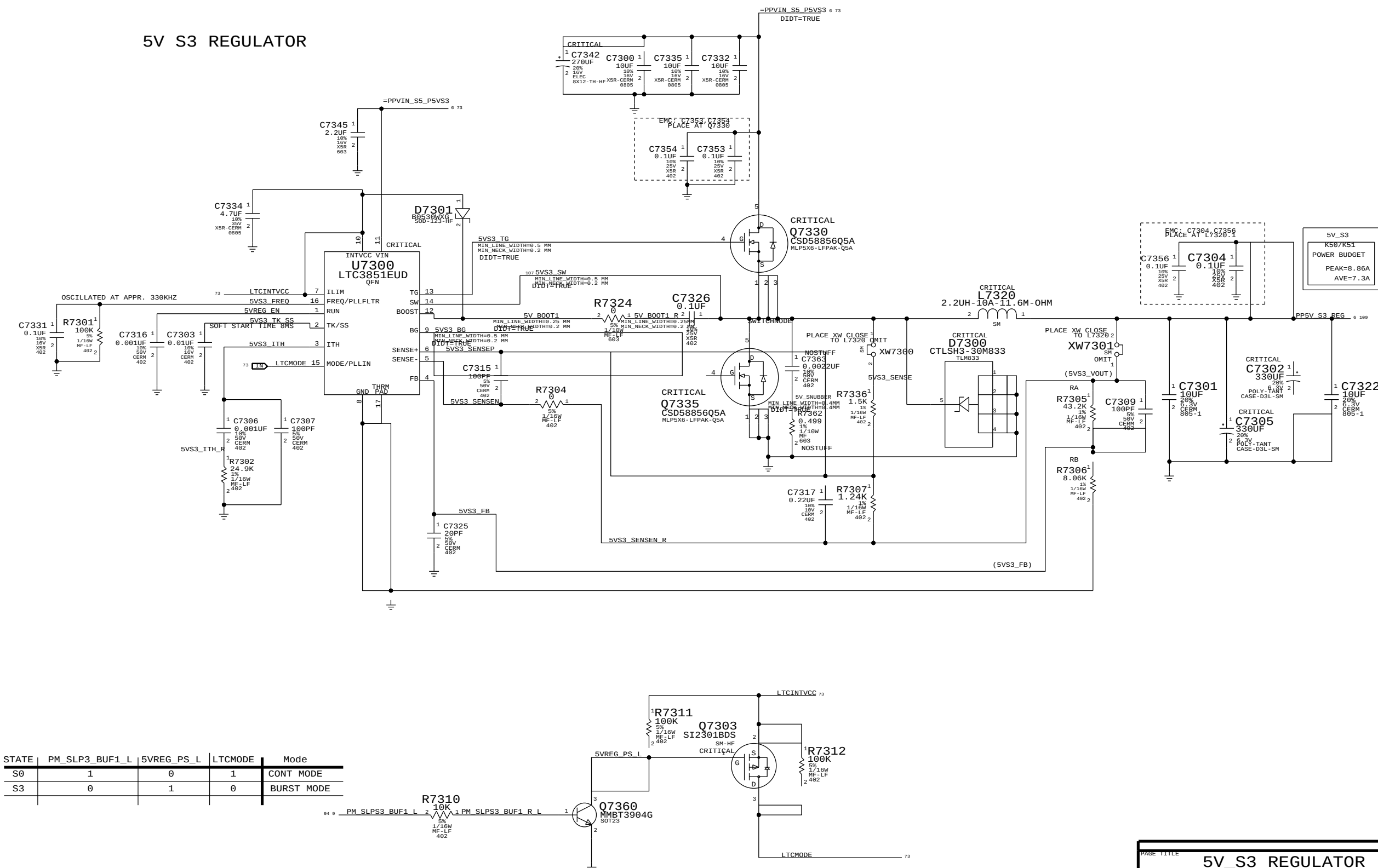
State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0







5V S3 REGULATOR



STATE	PM_SLP3_BUF1_L	5VREG_PS_L	LTCMODE	Mode
S0	1	0	1	CONT MODE
S3	0	1	0	BURST MODE

PAGE TITLE

5V_S3 REGULATOR

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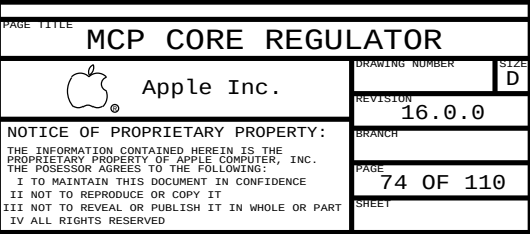
16.0.0

REVISION

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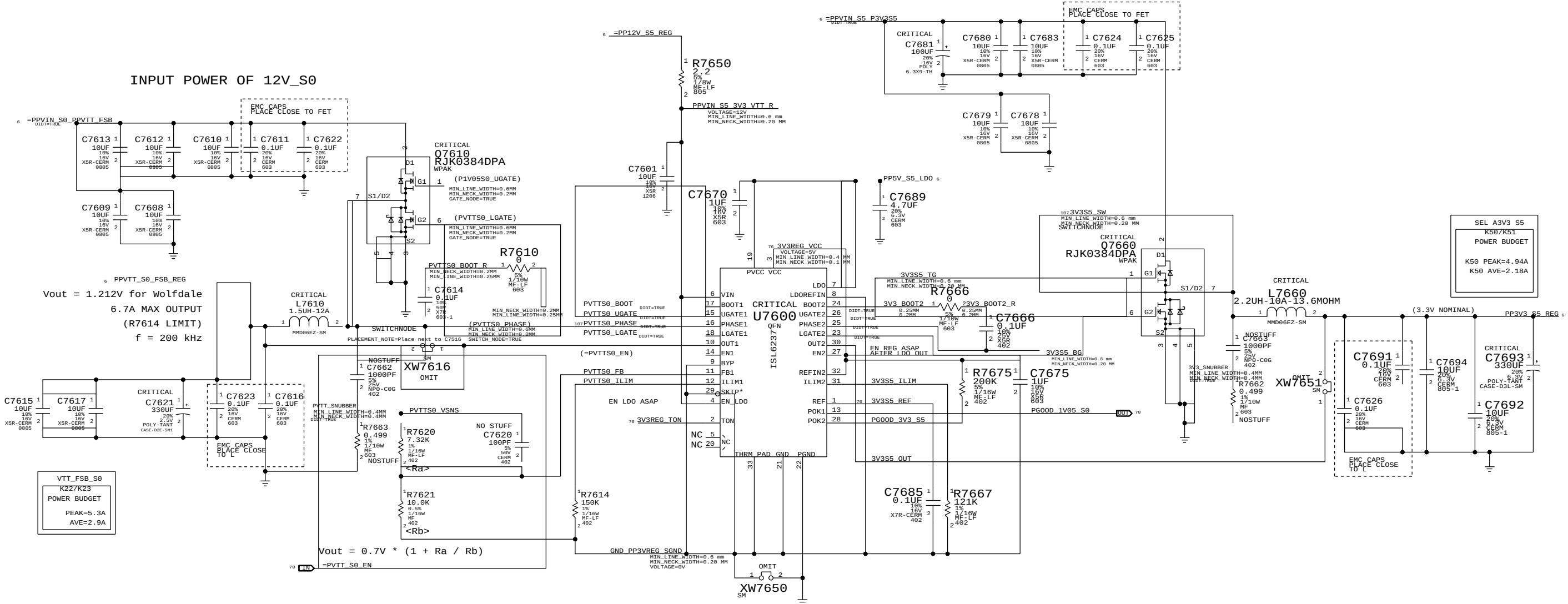
SHEET



FSB VTT AND 3.3V S5 RAILS

INPUT POWER OF 12V_S5

INPUT POWER OF 12V_S0



EN LDO TIED TO 12V_S5 TO EN LDO FIRST & REGULATOR INTERNAL LOGIC GETS POWER
 EN2 (3V3_S5) IS TIED TO VCC, TIED INTERNALLY TO PVCC
 TIED EXTERNALLY TO LDO OUT, SO REGULATOR IS ENABLED
 AS SOON AS LDO OUTPUT IS GOOD

EN1 (PPVTT_S0) CONTROLLED SEPARATELY

FSB VTT/3.3V S5 SUPPLIES			
	DRAWING NUMBER	16.0.0	SIZE D
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(ENABLED AT 2,8V MINIMUM)

CRITICAL
 L7920
 2.2uH-3.25A
 IHLP1616BZ-SM

CRITICAL
 U7950
 TPS62510

CRITICAL
 L7980
 51.1K

CRITICAL
 L7981
 60.4K

VOUT = 0.6V * (1 + Ra / Rb)

Vout = 1.1V
 MAX Current = 1.5A
 FREQ = 1Mhz

PAGE TITLE		1v1 S5 POWER SUPPLY	
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	8	7	6	5	4	3	2	1	
D									D
C									C
B									B
A									A
	8	7	6	5	4	3	2	1	

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[illegible]

[illegible]

[illegible]

Power aliases required by this page:

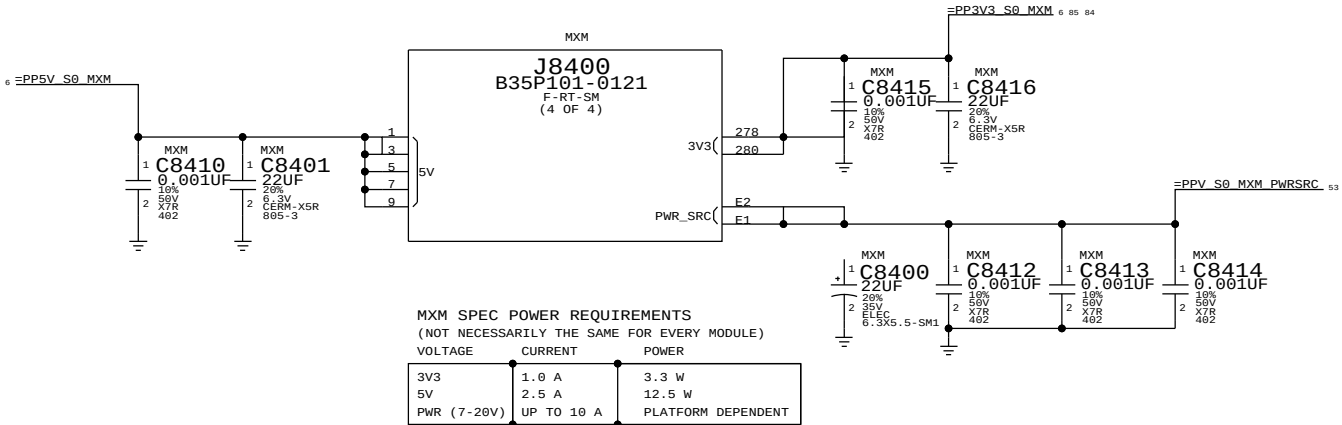
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

- MXM

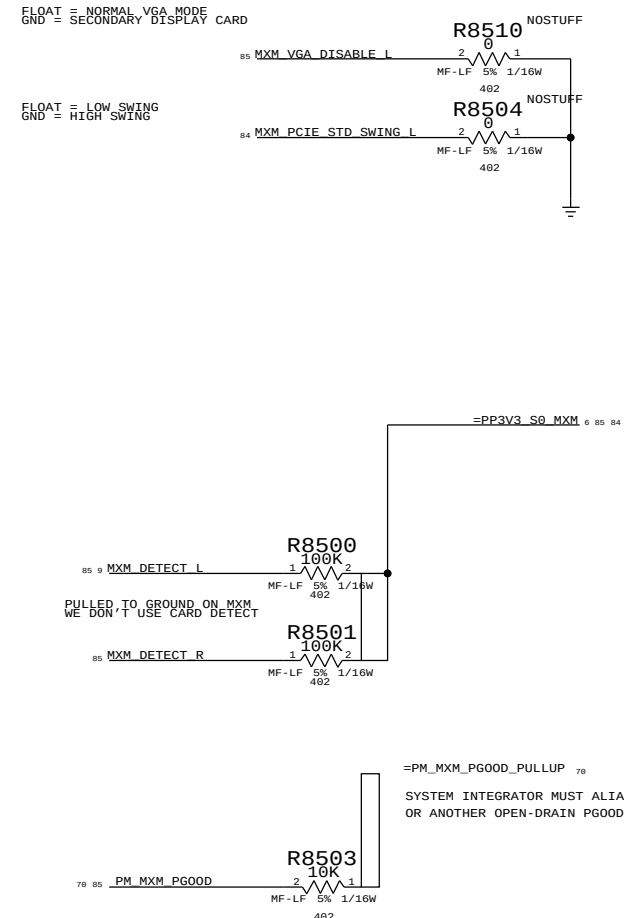


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MXM PCiE, DP & Power		SIZE D	
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BOM options provided by this page:

PULLUPS & PULLDOWNS AT MXM CONNECTOR

[illegible]

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Page Notes

Power aliases required by this page:
- =PP3V3_S0_DP

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

MCP Connections

84	CLK_100M_MXM_P	==	GPU_CLK100M_PCIE_P	9 101
			MAKE_BASE=TRUE	
84	CLK_100M_MXM_N	==	GPU_CLK100M_PCIE_N	9 101
			MAKE_BASE=TRUE	
84	MXM_RESET_L	==	PEG_RESET_L	9
			MAKE_BASE=TRUE	

Unused LVDS Interfaces

10	LVDS_IG_A_CLK_P	==	NC_LVDS_IG_A_CLK_P	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	LVDS_IG_A_CLK_N	==	NC_LVDS_IG_A_CLK_N	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	LVDS_IG_A_DATA_P<0>	==	NC_LVDS_IG_A_DATA_P<0>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	LVDS_IG_A_DATA_N<0>	==	NC_LVDS_IG_A_DATA_N<0>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	LVDS_IG_A_DATA_P<1>	==	NC_LVDS_IG_A_DATA_P<1>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	LVDS_IG_A_DATA_N<1>	==	NC_LVDS_IG_A_DATA_N<1>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	LVDS_IG_A_DATA_P<2>	==	NC_LVDS_IG_A_DATA_P<2>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	LVDS_IG_A_DATA_N<2>	==	NC_LVDS_IG_A_DATA_N<2>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	LVDS_IG_A_DATA_P<3>	==	NC_LVDS_IG_A_DATA_P<3>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	LVDS_IG_A_DATA_N<3>	==	NC_LVDS_IG_A_DATA_N<3>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	LVDS_IG_B_CLK_P	==	NC_LVDS_IG_B_CLK_P	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	LVDS_IG_B_CLK_N	==	NC_LVDS_IG_B_CLK_N	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	LVDS_IG_B_DATA_P<0>	==	NC_LVDS_IG_B_DATA_P<0>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	LVDS_IG_B_DATA_N<0>	==	NC_LVDS_IG_B_DATA_N<0>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	LVDS_IG_B_DATA_P<1>	==	NC_LVDS_IG_B_DATA_P<1>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	LVDS_IG_B_DATA_N<1>	==	NC_LVDS_IG_B_DATA_N<1>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	LVDS_IG_B_DATA_P<2>	==	NC_LVDS_IG_B_DATA_P<2>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	LVDS_IG_B_DATA_N<2>	==	NC_LVDS_IG_B_DATA_N<2>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	LVDS_IG_B_DATA_P<3>	==	NC_LVDS_IG_B_DATA_P<3>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	LVDS_IG_B_DATA_N<3>	==	NC_LVDS_IG_B_DATA_N<3>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	LVDS_IG_DDC_CLK	==	NC_LVDS_IG_DDC_CLK	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	LVDS_IG_DDC_DATA	==	NC_LVDS_IG_DDC_DATA	NO_TEST=TRUE
			MAKE_BASE=TRUE	

Unused MXM Interfaces

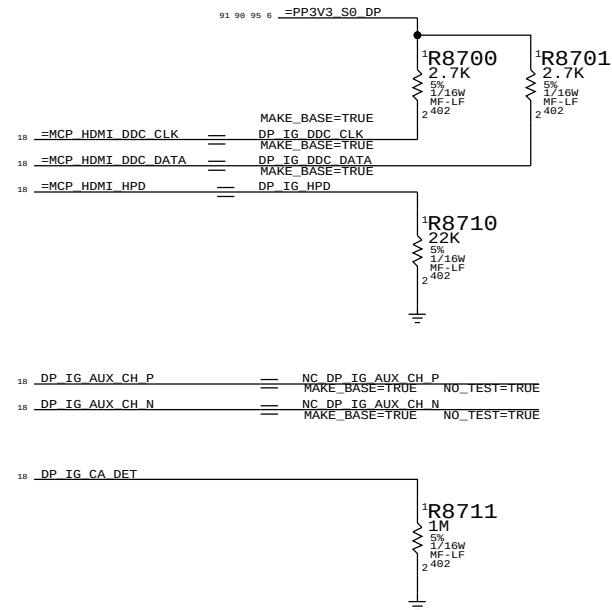
85	MXM_LVDS_A_CLK_N	==	NC_MXM_LVDS_A_CLK_N	NO_TEST=TRUE
			MAKE_BASE=TRUE	
85	MXM_LVDS_A_CLK_P	==	NC_MXM_LVDS_A_CLK_P	NO_TEST=TRUE
			MAKE_BASE=TRUE	
85	MXM_LVDS_A_DATA_N<0>	==	NC_MXM_LVDS_A_DATA_N<0>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
85	MXM_LVDS_A_DATA_P<0>	==	NC_MXM_LVDS_A_DATA_P<0>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
85	MXM_LVDS_A_DATA_N<1>	==	NC_MXM_LVDS_A_DATA_N<1>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
85	MXM_LVDS_A_DATA_P<1>	==	NC_MXM_LVDS_A_DATA_P<1>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
85	MXM_LVDS_A_DATA_N<2>	==	NC_MXM_LVDS_A_DATA_N<2>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
85	MXM_LVDS_A_DATA_P<2>	==	NC_MXM_LVDS_A_DATA_P<2>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
85	MXM_LVDS_A_DATA_N<3>	==	NC_MXM_LVDS_A_DATA_N<3>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
85	MXM_LVDS_A_DATA_P<3>	==	NC_MXM_LVDS_A_DATA_P<3>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
85	MXM_LVDS_B_CLK_N	==	NC_MXM_LVDS_B_CLK_N	NO_TEST=TRUE
			MAKE_BASE=TRUE	
85	MXM_LVDS_B_CLK_P	==	NC_MXM_LVDS_B_CLK_P	NO_TEST=TRUE
			MAKE_BASE=TRUE	
85	MXM_LVDS_B_DATA_N<0>	==	NC_MXM_LVDS_B_DATA_N<0>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
85	MXM_LVDS_B_DATA_P<0>	==	NC_MXM_LVDS_B_DATA_P<0>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
85	MXM_LVDS_B_DATA_N<1>	==	NC_MXM_LVDS_B_DATA_N<1>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
85	MXM_LVDS_B_DATA_P<1>	==	NC_MXM_LVDS_B_DATA_P<1>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
85	MXM_LVDS_B_DATA_N<2>	==	NC_MXM_LVDS_B_DATA_N<2>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
85	MXM_LVDS_B_DATA_P<2>	==	NC_MXM_LVDS_B_DATA_P<2>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
85	MXM_LVDS_B_DATA_N<3>	==	NC_MXM_LVDS_B_DATA_N<3>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
85	MXM_LVDS_B_DATA_P<3>	==	NC_MXM_LVDS_B_DATA_P<3>	NO_TEST=TRUE
			MAKE_BASE=TRUE	

Unused MXM DP Interfaces

84	MXM_DP_B_ML_P<0...3>	==	NC_MXM_DP_B_ML_P<0...3>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
84	MXM_DP_B_ML_N<0...3>	==	NC_MXM_DP_B_ML_N<0...3>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
84	MXM_DP_B_AUX_P	==	NC_MXM_DP_B_AUX_P	NO_TEST=TRUE
			MAKE_BASE=TRUE	
84	MXM_DP_B_AUX_N	==	NC_MXM_DP_B_AUX_N	NO_TEST=TRUE
			MAKE_BASE=TRUE	
84	MXM_DP_B_HPD	==	NC_MXM_DP_B_HPD	NO_TEST=TRUE
			MAKE_BASE=TRUE	
84	MXM_DP_D_ML_P<0...3>	==	NC_MXM_DP_D_ML_P<0...3>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
84	MXM_DP_D_ML_N<0...3>	==	NC_MXM_DP_D_ML_N<0...3>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
84	MXM_DP_D_AUX_P	==	NC_MXM_DP_D_AUX_P	NO_TEST=TRUE
			MAKE_BASE=TRUE	
84	MXM_DP_D_AUX_N	==	NC_MXM_DP_D_AUX_N	NO_TEST=TRUE
			MAKE_BASE=TRUE	
84	MXM_DP_D_HPD	==	NC_MXM_DP_D_HPD	NO_TEST=TRUE
			MAKE_BASE=TRUE	

Unused MCP Interfaces

10	LVDS_IG_BKL_ON	==	NC_LVDS_IG_BKL_ON	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	LVDS_IG_BKL_PWM	==	NC_LVDS_IG_BKL_PWM	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	LVDS_IG_PANEL_PWR	==	NC_LVDS_IG_PANEL_PWR	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	=MCP_HDMI_TXD_P<0...2>	==	NC_MCP_HDMI_TXD_P<0...2>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	=MCP_HDMI_TXD_N<0...2>	==	NC_MCP_HDMI_TXD_N<0...2>	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	=MCP_HDMI_TXC_P	==	NC_MCP_HDMI_TXC_P	NO_TEST=TRUE
			MAKE_BASE=TRUE	
10	=MCP_HDMI_TXC_N	==	NC_MCP_HDMI_TXC_N	NO_TEST=TRUE
			MAKE_BASE=TRUE	



PAGE TITLE		Display: Aliases	
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Page Notes

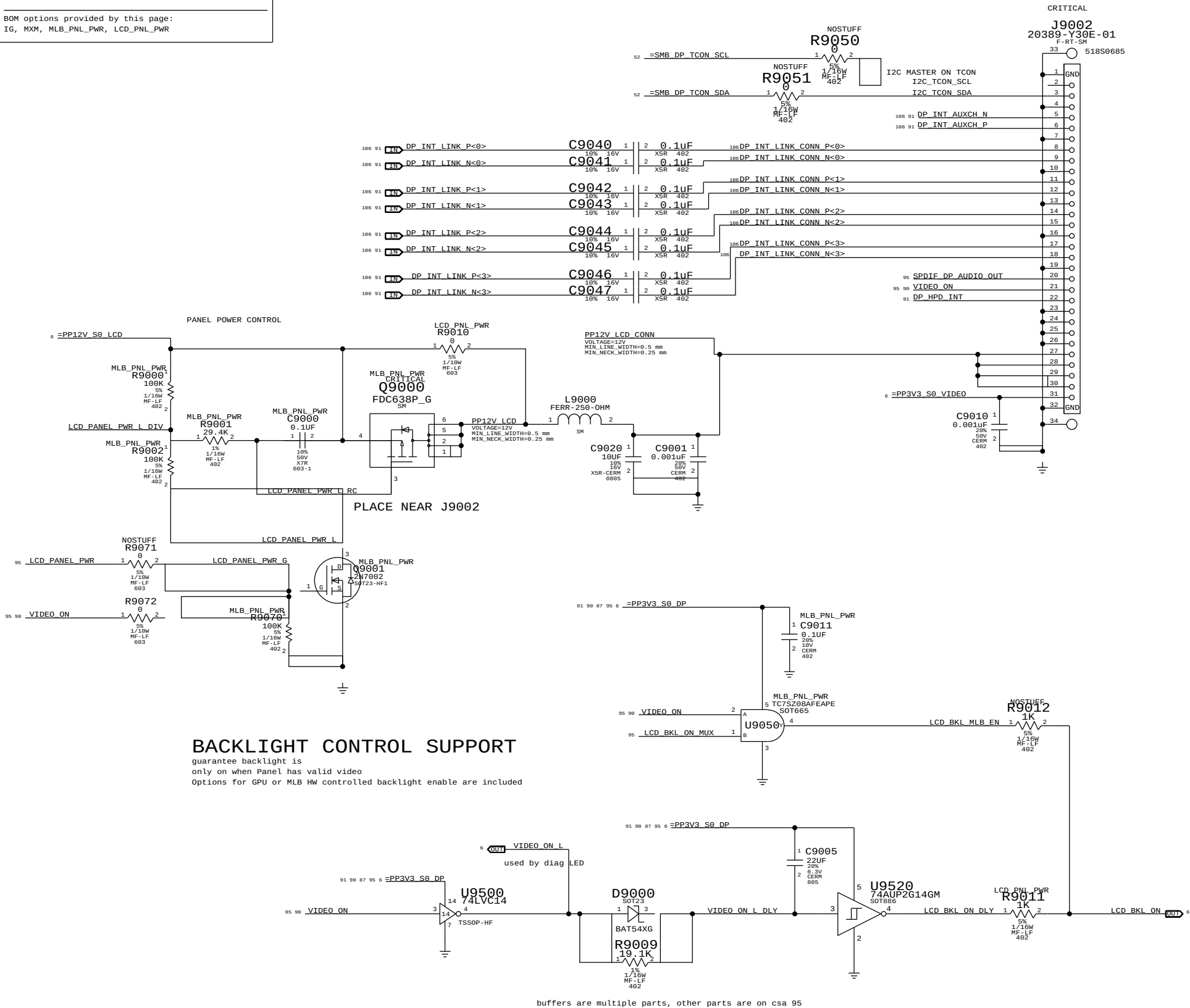
Power aliases required by this page:

- =PP12V_S0_LCD
- =PP3V3_S0_VIDEO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
IG, MXM, MLB_PNL_PWR, LCD_PNL_PWR

INTERNAL DP INTERFACE



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Display: Int DP Connector	
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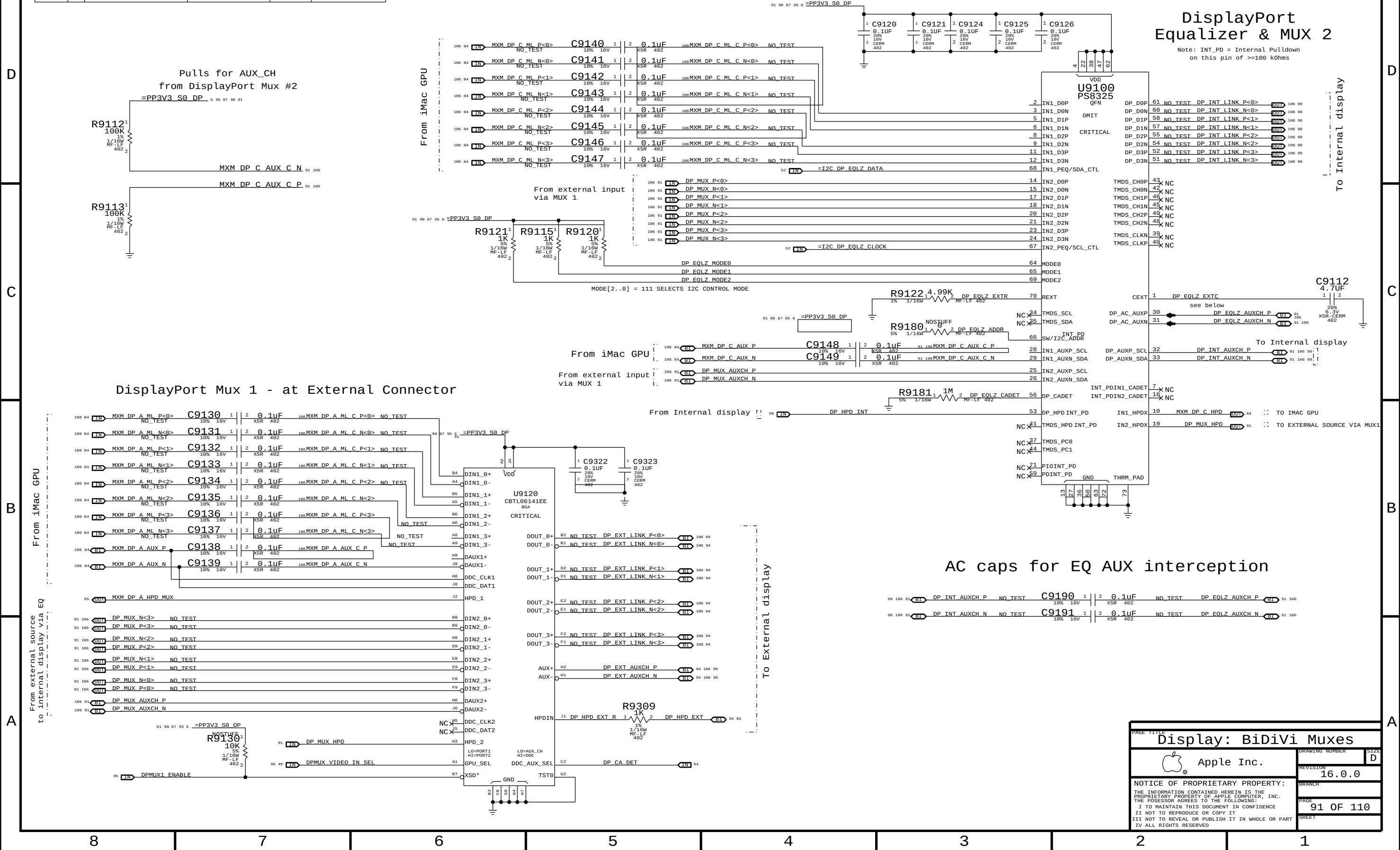
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0752	1	IC, PS8325, DP MUX, EQ	U9100	CRITICAL	

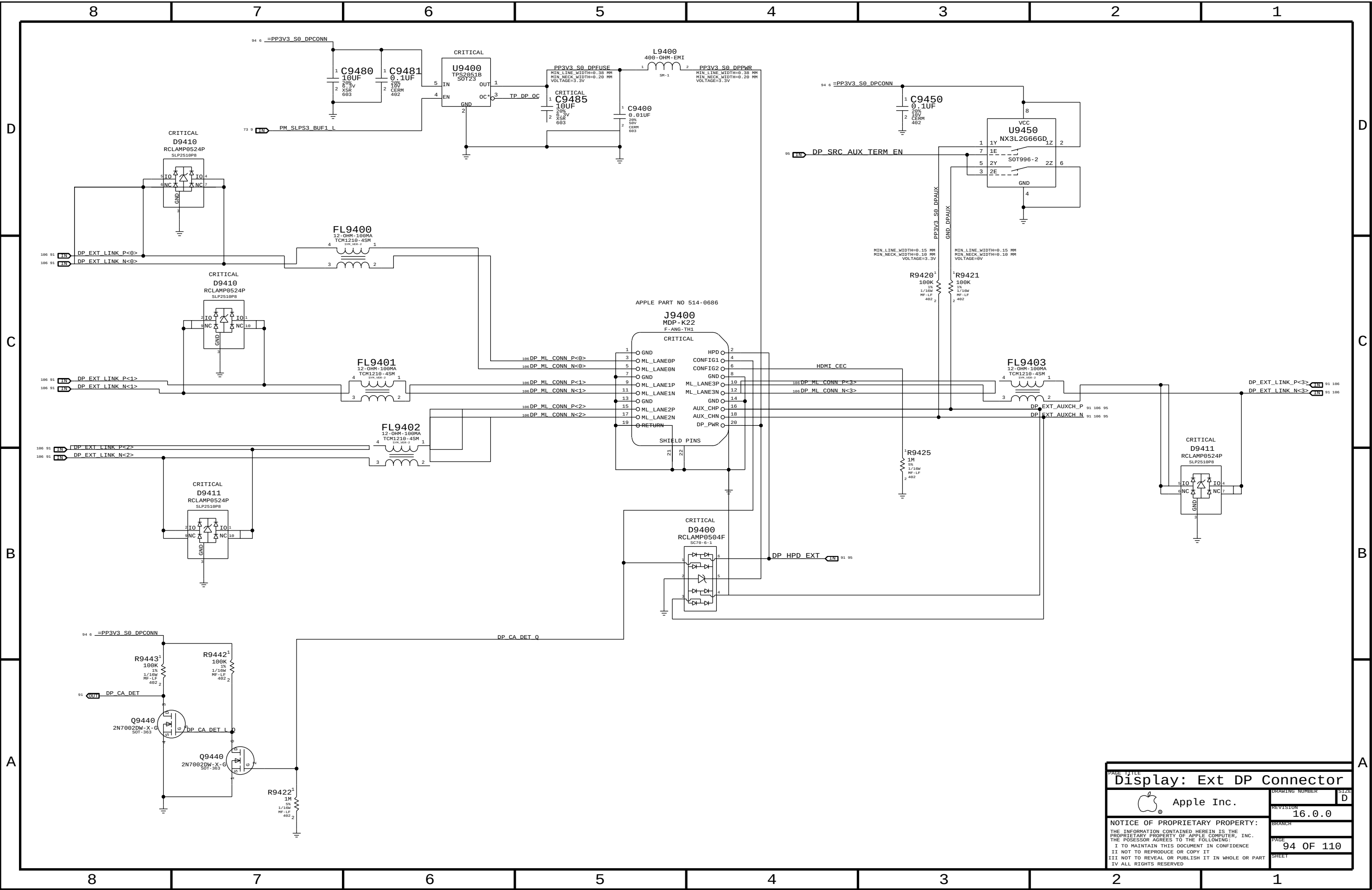


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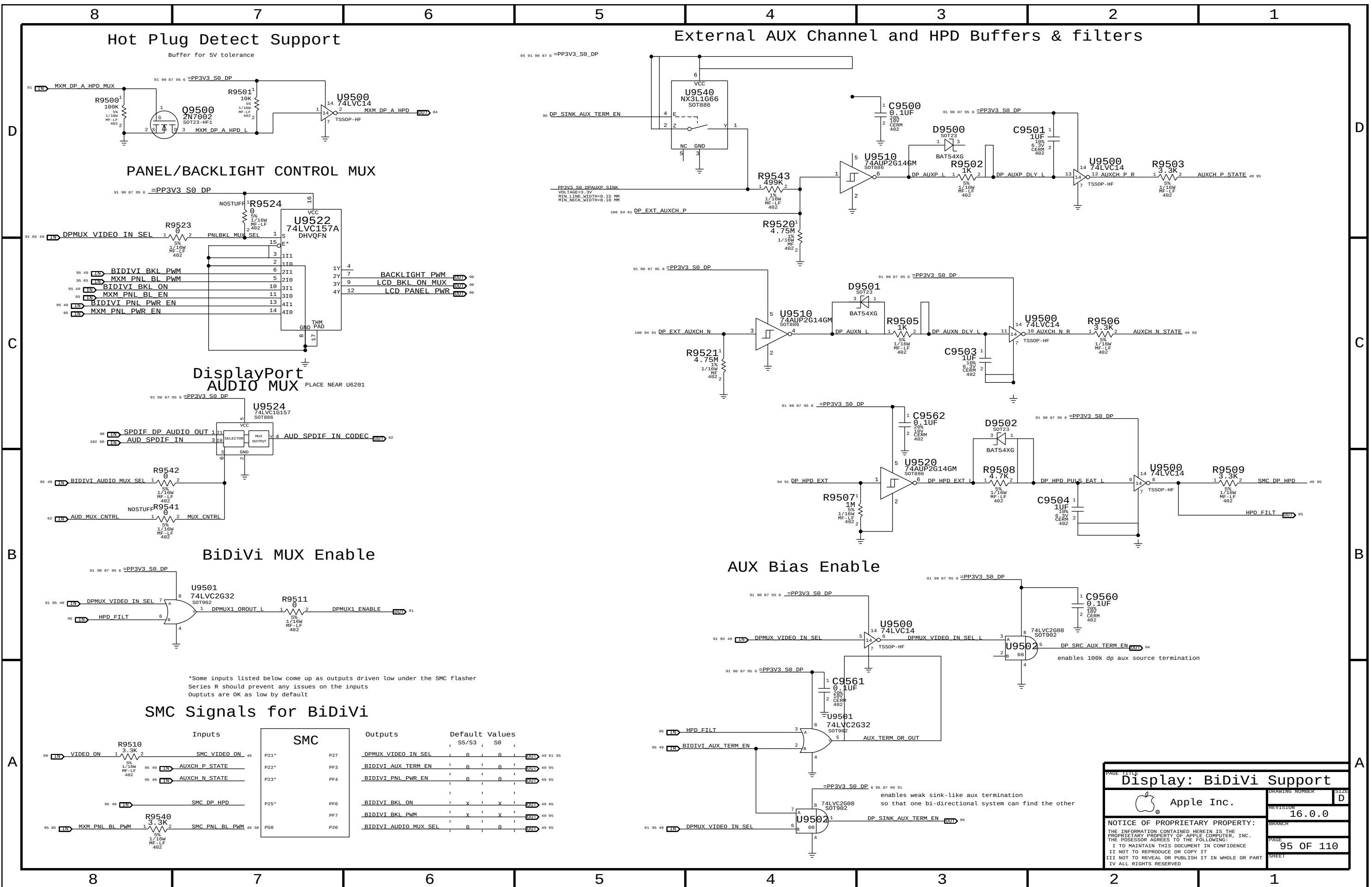
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SR DG recommends at least 25 mils, >50 mils preferred

MCP FSB COMP Signal Constraints

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

CPU / FSB Net Properties

FSB 4X Signal Groups

FSB 2X
Signals

FSB 1X Signals

A

8

7

6

5

4

3

2

1

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_20THER	*	=3:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
MCP_MEM_COMP	*	Y	0.175 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
MCP_MEM_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
	MEM_70D_VDD	MEM_CLK	MEM A CLK P<1..0>	15 33
	MEM_70D_VDD	MEM_CLK	MEM A CLK N<1..0>	15 33
	MEM_70D_VDD	MEM_CLK	MEM A CLK P<4..3>	16 33
	MEM_70D_VDD	MEM_CLK	MEM A CLK N<4..3>	16 33
	MEM_40S_VDD	MEM_CTRL	MEM A CKE<3..0>	15 16 31
	MEM_40S_VDD	MEM_CTRL	MEM A CS L<3..0>	15 16 31
	MEM_40S_VDD	MEM_CTRL	MEM A ODT<3..0>	15 16 31
	MEM_40S_VDD	MEM_CMD	MEM A A<14..0>	15 31
	MEM_40S_VDD	MEM_CMD	MEM A BA<2..0>	15 31
	MEM_40S_VDD	MEM_CMD	MEM A RAS L	15 31
	MEM_40S_VDD	MEM_CMD	MEM A CAS L	15 31
	MEM_40S_VDD	MEM_CMD	MEM A WE L	15 31
	MEM_40S	MEM_DATA	MEM A DQ<7..0>	15 33
	MEM_40S	MEM_DATA	MEM A DM<0>	15 33
	MEM_40S	MEM_DATA	MEM A DQ<15..8>	15 33
	MEM_40S	MEM_DATA	MEM A DM<1>	15 33
	MEM_40S	MEM_DATA	MEM A DQ<23..16>	15 33
	MEM_40S	MEM_DATA	MEM A DM<2>	15 33
	MEM_40S	MEM_DATA	MEM A DQ<31..24>	15 33
	MEM_40S	MEM_DATA	MEM A DM<3>	15 33
	MEM_40S	MEM_DATA	MEM A DQ<39..32>	15 33
	MEM_40S	MEM_DATA	MEM A DM<4>	15 33
	MEM_40S	MEM_DATA	MEM B CLK P<1..0>	15 33
	MEM_70D_VDD	MEM_CLK	MEM B CLK N<1..0>	15 33
	MEM_70D_VDD	MEM_CLK	MEM B CLK P<4..3>	16 33
	MEM_70D_VDD	MEM_CLK	MEM B CLK N<4..3>	16 33
	MEM_40S_VDD	MEM_CTRL	MEM B CKE<3..0>	15 16 32
	MEM_40S_VDD	MEM_CTRL	MEM B CS L<3..0>	15 16 32
	MEM_40S_VDD	MEM_CTRL	MEM B ODT<3..0>	15 16 32
	MEM_40S_VDD	MEM_CMD	MEM B A<14..0>	15 32
	MEM_40S_VDD	MEM_CMD	MEM B BA<2..0>	15 32
	MEM_40S_VDD	MEM_CMD	MEM B RAS L	15 32
	MEM_40S_VDD	MEM_CMD	MEM B CAS L	15 32
	MEM_40S_VDD	MEM_CMD	MEM B WE L	15 32
	MEM_40S	MEM_DATA	MEM B DQ<7..0>	15 33
	MEM_40S	MEM_DATA	MEM B DM<0>	15 33
	MEM_40S	MEM_DATA	MEM B DQ<15..8>	15 33
	MEM_40S	MEM_DATA	MEM B DM<1>	15 33
	MEM_40S	MEM_DATA	MEM B DQ<23..16>	15 33
	MEM_40S	MEM_DATA	MEM B DM<2>	15 33
	MEM_40S	MEM_DATA	MEM B DQ<31..24>	15 33
	MEM_40S	MEM_DATA	MEM B DM<3>	15 33
	MEM_40S	MEM_DATA	MEM B DQ<39..32>	15 33
	MEM_40S	MEM_DATA	MEM B DM<4>	15 33
	MEM_40S	MEM_DATA	MEM B DQ<47..40>	15 33
	MEM_40S	MEM_DATA	MEM B DM<5>	15 33
	MEM_40S	MEM_DATA	MEM B DQ<55..48>	15 33
	MEM_40S	MEM_DATA	MEM B DM<6>	15 33
	MEM_40S	MEM_DATA	MEM B DQ<63..56>	15 33
	MEM_40S	MEM_DATA	MEM B DM<7>	15 33

PCI-Express

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	0.5 MM	?
MCP_PEX_COMP	*	0.2 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SATA Interface Constraints

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERM	*	0.2 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
PHYSICAL		SPACING		
PCIE GRAPHICS				
□	PCIE_900	PCIE	PEG R2D C P<15..0>	9 86
□	PCIE_900	PCIE	PEG R2D C N<15..0>	9 86
□	PCIE_900	PCIE	PEG D2R P<15..0>	86 9
□	PCIE_900	PCIE	PEG D2R N<15..0>	86 9
□	PCIE_900	PCIE	MXM PCIE R2D P<15..0>	86 84
□	PCIE_900	PCIE	MXM PCIE R2D N<15..0>	86 84
□	PCIE_900	PCIE	MXM PCIE D2R P<15..0>	84 86
□	PCIE_900	PCIE	MXM PCIE D2R N<15..0>	84 86
PCIE I/O				
□	PCIE_900	PCIE	PCIE MINI R2D P	34
□	PCIE_900	PCIE	PCIE MINI R2D N	34
□	PCIE_900	PCIE	PCIE MINI R2D C P	17 34
□	PCIE_900	PCIE	PCIE MINI R2D C N	17 34
□	PCIE_900	PCIE	PCIE MINI R2D I P	34
□	PCIE_900	PCIE	PCIE MINI R2D I N	34
□	PCIE_900	PCIE	PCIE MINI D2R P	34 17
□	PCIE_900	PCIE	PCIE MINI D2R N	34 17
□	PCIE_900	PCIE	PCIE FW R2D P	41
□	PCIE_900	PCIE	PCIE FW R2D N	41
□	PCIE_900	PCIE	PCIE FW R2D C P	17 41
□	PCIE_900	PCIE	PCIE FW R2D C N	17 41
□	PCIE_900	PCIE	PCIE FW D2R P	41 17
□	PCIE_900	PCIE	PCIE FW D2R N	41 17
□	PCIE_900	PCIE	PCIE FW D2R C P	41
□	PCIE_900	PCIE	PCIE FW D2R C N	41
PCIE REF CLOCKS				
□	CLK PCIE 1000	CLK PCIE	GPU CLK100M PCIE P	9 87
□	CLK PCIE 1000	CLK PCIE	GPU CLK100M PCIE N	9 87
□	CLK PCIE 1000	CLK PCIE	PCIE CLK100M MINI P	17 34
□	CLK PCIE 1000	CLK PCIE	PCIE CLK100M MINI N	17 34
□	CLK PCIE 1000	CLK PCIE	PCIE CLK100M MINI CON P	34
□	CLK PCIE 1000	CLK PCIE	PCIE CLK100M MINI CON N	34
□	CLK PCIE 1000	CLK PCIE	PCIE CLK100M FW P	17 41
□	CLK PCIE 1000	CLK PCIE	PCIE CLK100M FW N	17 41
SATA				
□	SATA_1000	SATA	SATA HDD R2D C P	20 45
□	SATA_1000	SATA	SATA HDD R2D C N	20 45
□	SATA_1000	SATA	SATA HDD R2D P	45 10
□	SATA_1000	SATA	SATA HDD R2D N	45 10
□	SATA_1000	SATA	SATA HDD D2R P	45 20
□	SATA_1000	SATA	SATA HDD D2R N	45 20
□	SATA_1000	SATA	SATA HDD D2R C P	45 10
□	SATA_1000	SATA	SATA HDD D2R C N	45 10
□	SATA_1000	SATA	SATA ODD R2D C P	20 45
□	SATA_1000	SATA	SATA ODD R2D C N	20 45
□	SATA_1000	SATA	SATA ODD R2D P	45 10
□	SATA_1000	SATA	SATA ODD R2D N	45 10
□	SATA_1000	SATA	SATA ODD D2R P	45 20
□	SATA_1000	SATA	SATA ODD D2R N	45 20
□	SATA_1000	SATA	SATA ODD D2R C P	45 10
□	SATA_1000	SATA	SATA ODD D2R C N	45 10
□	MCP_SBS	SATA_TERM0	MCP SATA_TERM0	20
MISC				
□	MCP_SBS	MCP_PEX_COMP	MCP_PEX_CLK_COMP	17
□	MCP_IV_COMP	MCP_PEX_COMP	MCP_IFPAB_RSET	10 26
□	MCP_SBS	MCP_PEX_COMP	MCP_IFPAB_VPROBE	10 26
□			PM_SLP_S3_L	21 9
□			PM_SLP_S4_L	21 70

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v00), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

XTAL Constraints

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
	PCT 55S	PCT	PCI REQ0 L	19
	PCT 55S	PCT	PCI REQ1 L	19
	CLK PCT 55S	CLK PCT	PCI CLK33M MCP R	19
	CLK PCT 55S	CLK PCT	PCI CLK33M MCP	19
	LPC 55S	LPC	LPC AD<3..0>	19 40 51
	LPC 55S	LPC	LPC AD R<3..0>	19
	LPC 55S	LPC	LPC FRAME L	19 40 51
	LPC 55S	LPC	LPC FRAME R L	19
	LPC 55S	LPC	LPC RESET L	19 9
	CLK LPC 55S	CLK LPC	LPC CLK33M SMC R	19 9
	CLK LPC 55S	CLK LPC	LPC CLK33M SMC	9 49
	CLK LPC 55S	CLK LPC	LPC CLK33M LPCPLUS	9 51
	CLK LPC 55S	CLK LPC	PM CLK32K SUSCLK R	21 9
	CLK LPC 55S	CLK LPC	PM CLK32K SUSCLK	9 49
	MCP USB RBTAS		MCP USB RBTAS GND	20
	USB 980	USB	USB EXT_A_P	20 46
	USB 980	USB	USB EXT_A_N	20 46
	USB 980	USB	USB PORT0_P	46
	USB 980	USB	USB PORT0_N	46
	USB 980	USB	USB EXT_B_P	20 46
	USB 980	USB	USB EXT_B_N	20 46
	USB 980	USB	USB PORT1_P	46
	USB 980	USB	USB PORT1_N	46
	USB 980	USB	USB EXT_C_P	20 46
	USB 980	USB	USB EXT_C_N	20 46
	USB 980	USB	USB PORT2_P	46
	USB 980	USB	USB PORT2_N	46
	USB 980	USB	USB EXT_D_P	20 46
	USB 980	USB	USB EXT_D_N	20 46
	USB 980	USB	USB D_MUXED_P	46
	USB 980	USB	USB D_MUXED_N	46
	USB 980	USB	USB PORT3_P	46
	USB 980	USB	USB PORT3_N	46
	USB 980	USB	USB CAMERA_P	20 47
	USB 980	USB	USB CAMERA_N	20 47
	USB 980	USB	USB CAMERA_L_P	47 109
	USB 980	USB	USB CAMERA_L_N	47 109
	USB 980	USB	USB_BT_P	20 47
	USB 980	USB	USB_BT_N	20 47
	USB 980	USB	USB_BT_L_P	47 109
	USB 980	USB	USB_BT_L_N	47 109
	USB 980	USB	USB_IR_P	20 47
	USB 980	USB	USB_IR_N	20 47
	USB 980	USB	USB_IR_L_P	47 109
	USB 980	USB	USB_IR_L_N	47 109
	USB 980	USB	USB_SDCARD_P	20 47
	USB 980	USB	USB_SDCARD_N	20 47
	USB 980	USB	USB_SDCARD_L_P	47 109
	USB 980	USB	USB_SDCARD_L_N	47 109
	MCP 58S	SPI	SPI_CLK_R	21 51 61
	MCP 58S	SPI	SPI_CLK	61
	MCP 58S	SPI	SPI_MOSI_R	21 51 61
	MCP 58S	SPI	SPI_MOSI	61
	MCP 58S	SPI	SPI_MISO	51 61 21
	MCP 58S	SPI	SPI_MISO_R	61
	MCP 58S	SPI	SPI_CS0_R_L	21 51
	MCP 58S	SPI	SPI_CS0_L	51
	HDA 55S	HDA	HDA_BIT_CLK	21 62
		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	21
	HDA 55S	HDA	HDA_BIT_CLK_R	21
	HDA 55S	HDA	HDA_RST_L	21 62
	HDA 55S	HDA	HDA_RST_R_L	21
	HDA 55S	HDA	HDA_SDOUT	21 62
	HDA 55S	HDA	HDA_SDOUT_R	21
	HDA 55S	HDA	HDA_SYNC	21 62
	HDA 55S	HDA	HDA_SYNC_R	21
	HDA 55S	HDA	HDA_SDIN0	62 21
	HDA 55S	HDA	AUD_SDI_R	62
		HDA	AUD_SPDIF_IN	66 95
		HDA	AUD_SPDIF_OUT	62 66
		HDA	AUD_SPDIF_CHIP	62
	CLK MCP_XTAL	XTAL	MCP_CLK25M_XTALOUT	21 20
	CLK MCP_XTAL	XTAL	MCP_CLK25M_XTALIN	20 21
	CLK MCP_XTAL	XTAL	RTC_CLK32K_XTALOUT	21 20
	CLK MCP_XTAL	XTAL	RTC_CLK32K_XTALIN	20 21

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
ENET_MII_555	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	0.3 MM	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

RTL8211CLGR (ETHERNET PHY) CONSTRAINTS

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
		MCP_MII_COMP		MCP_MII_COMP_VDD 18
		MCP_MII_COMP		MCP_MII_COMP_GND 18
		ENET_MII_555	MCP_BUE0_CLK	MCP_CLK25M_BUE0_R 18
		ENET_MII_555	MCP_BUE0_CLK	RTL8211_CLK25M_CKXTAL1 38 37
		ENET_MII_555	ENET_MII	ENET_MDIO 18 37
		ENET_MII_555	ENET_MII	ENET_MDC 18 37
		ENET_MII_555	ENET_MII	ENET_CLK125M_RXCLK 37 18
		ENET_MII_555	ENET_MII	ENET_CLK125M_RXCLK_R 37
		ENET_MII_555	ENET_MII	ENET_RXD<0> 37 18
		ENET_MII_555	ENET_MII	ENET_RXD_R<0> 37
		ENET_MII_555	ENET_MII	ENET_RXD<3..1> 37 18
		ENET_MII_555	ENET_MII	ENET_RXD_R<3..1> 37 18
		ENET_MII_555	ENET_MII	ENET_RX_CTRL 37 18
		ENET_MII_555	ENET_MII	ENET_RXCTL_R 37
		ENET_MII_555	ENET_MII	ENET_CLK125M_TXCLK 18 37
		ENET_MII_555	ENET_MII	ENET_TXD<0> 18 37
		ENET_MII_555	ENET_MII	ENET_TXD<3..1> 18 37
		ENET_MII_555	ENET_MII	ENET_TX_CTRL 18 37
		ENET_MDI_1000	ENET_MDI	ENET_MDI_P<3..0> 18 27
		ENET_MDI_1000	ENET_MDI	ENET_MDI_N<3..0> 37 29
		ENET_MDI_1000	ENET_MDI	ENET_MDI_T_P<3..0> 37 29
		ENET_MDI_1000	ENET_MDI	ENET_MDI_T_N<3..0> 39

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
	SMB_55S	GMR	SMBUS SMC A S3_SCL	52
	SMB_55S	GMR	SMBUS SMC A S3_SDA	52
	SMB_55S	GMR	SMBUS SMC B S0_SCL	52
	SMB_55S	GMR	SMBUS SMC B S0_SDA	52
	SMB_55S	GMR	SMBUS SMC 0 S0_SCL	52
	SMB_55S	GMR	SMBUS SMC 0 S0_SDA	52
	SMB_55S	GMR	SMBUS SMC BSA_SCL	52
	SMB_55S	GMR	SMBUS SMC BSA_SDA	52
	SMB_55S	GMR	SMBUS SMC MGMT_SCL	105 52
	SMB_55S	GMR	SMBUS SMC MGMT_SDA	105 52
	SMB_55S	GMR	SMBUS SMC MGMT_SCL	105 52
	SMB_55S	GMR	SMBUS SMC MGMT_SDA	105 52
	SMB_55S	GMR	SMBUS MCP 0_CLK	13 21 52
	SMB_55S	GMR	SMBUS MCP 0_DATA	13 21 52

SMC Constraints

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SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SPACING_0.5MM	*	0.5 MM	?
CLK_SPACING_0.6MM	*	0.6 MM	?
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.6 MM	1000

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P1MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P1MM
CLK_LPC	*	BGA_P1MM	BGA_P1MM
CLK_PCI	*	BGA_P1MM	BGA_P1MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MCP_FSB_COMP	*	BGA_P1MM	BGA_P2MM
MCP_MEM_COMP	*	BGA_P1MM	BGA_P2MM
MCP_PEX_COMP	*	BGA_P1MM	BGA_P2MM

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	FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT								
D	J4700 USB CAMERA		J5520 ANALOG LCD TEMP SENSOR		J6601 AUDIO MICROPHONE				
	102 47	USB_CAMERA_L_P	55 107	SNS_LCD_P	66 66	AUD_MIC_IN1_N_CONN	GND 16 TP'S		
	102 47	USB_CAMERA_L_N	55 107	SNS_LCD_N	66 66	GND_AUDIO_MIC1_CONN	PP3V3_S3 2 TP'S		
	1 PP5V_S3_REG Testpoint near J4700				1 Ground Testpoint near J6601				
C	J4750 USB CARD READER		J5521 AMBIENT TEMP SENSOR		J6602 AUDIO RIGHT SPEAKER				
	102 47	USB_SDCARD_L_P	55 107	SNS_AMB_P	66 66	AUD_SPKR_OUTL02R_P	PP5V_S3_REG 2 TP'S		
	102 47	USB_SDCARD_L_N	55 107	SNS_AMB_N	66 66	AUD_SPKR_OUTL02R_N	PP5V_S0		
	1 PP3V3_S3 Testpoint near J4750				1 Ground Testpoint near J6601				
B	J4720 USB BLUETOOTH		J5551 ODD TEMP SENSOR		J6603 AUDIO LEFT SPEAKER				
	102 47	USB_BT_L_P	55 107	SNS_ODD_P	66 66	AUD_SPKR_OUTL02L_P			
	102 47	USB_BT_L_N	55 107	SNS_ODD_N	66 66	AUD_SPKR_OUTL02L_N			
	1 PP3V3_S3 Testpoint near J4720								
A	J4780 IR BOARD		J5600 ODD FAN						
	102 47	USB_IR_L_P	56 56	FAN_0_PWR_L					
	102 47	USB_IR_L_N	56 56	FAN_TACH0_L					
	1 PP5V_S3_REG Testpoint near J4780								
		J4520 SATA ODD (HIGH SPEED)		J5700 CPU FAN					
		45 101	SATA_ODD_R2D_P	57 57	FAN_2_PWR_L				
		45 101	SATA_ODD_R2D_N	57 57	FAN_TACH2_L				
		45 101	SATA_ODD_D2R_C_N	57 57	PP12V_S0_FAN2_L				
		45 101	SATA_ODD_D2R_C_P	57 57	FAN_2_GND				
		49 49	SMC_ODD_DETECT						
		1 PP5V_S0 Testpoint near J4520							
		5 Ground Testpoints near J4520							
		J4510 SATA HDD (HIGH SPEED)		J5601 HD FAN					
		101 45	SATA_HDD_R2D_P	56 56	FAN_1_PWR_L				
		101 45	SATA_HDD_R2D_N	56 56	FAN_TACH1_L				
		101 45	SATA_HDD_D2R_C_N	56 56	PP12V_S0_FAN1_L				
		101 45	SATA_HDD_D2R_C_P	56 56	FAN_1_GND				
		3 Ground Testpoints near J4510							
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